CH32V303/305/307/317 Datasheet

V3.5

https://wch-ic.com

Overview

CH32V series is an industrial-grade general-purpose microcontroller based on QingKe RISC-V core, including CH32V305 connected MCU, CH32V307/317 interconnected MCU, CH32V208 wireless MCU, etc. The CH32V30x and CH32V31x series is based on QingKe V4F microprocessor design, supports single-precision floating-point instruction and fast interrupt response, supports 144MHz main frequency zero-wait operation, provides 8 groups of U(S)ART, 4 groups of motor PWM advanced timers, SDIO, DVP, 4 groups of analog OPA, dual ADC units, dual DAC units, built-in USB2.0 high-speed PHY transceivers (480Mbps), Gigabit Ethernet MAC controller and 10M PHY transceivers, 10/100M PHY transceiver (CH32V317 only).

Features

- **Core:**

- QingKe 32-bit RISC-V4F core with multiple instruction set combinations
- Fast programmable interrupt controller + hardware interrupt stack
- Branch prediction, conflict handling mechanism
- Single cycle multiplication, hardware division, hardware FPU
- System main frequency 144MHz, zero wait

- **Memory:**

- Available with up to 128KB volatile data storage area SRAM
- Available with 480KB program memory CodeFlash (zero-wait application area + non-zero-wait data area)
- 28KB BootLoader
- 128B non-volatile system configuration memory
- 128B user-defined memory

- **Power management and low-power consumption:**

- System power supply V_{DD}: 3.3V
- Independent power supply for GPIO unit $V_{I/O}$: 3.3V
- Low-power mode: Sleep, Stop, Standby
- V_{BAT} independently powers RTC and backup register

- **Clock & Reset**

- Built-in factory-trimmed 8MHz RC oscillator
- Built-in about 40 kHz RC oscillator
- Built-in PLL, optional CPU clock up to 144MHz
- High-speed external 3~25MHz oscillator
- Low-speed external 32.768kHz oscillator
- Power on/down reset, programmable voltage detector

- **Real-time clock (RTC): 32-bit independent RTC timer**
- **2 groups of 18-channel general-purpose DMA controllers**

- 18 channels, support ring buffer
- Support TIMx/ADC/DAC/USART/I2C/SPI/I2S/SDIO

- **4 groups of OPAs and comparators: connected with ADC and TIMx**
- **2 groups of 12-bit DAC**
- **2 groups of 12-bit ADC**

- Analog input range: V_{SSA}~V_{DDA}
- 16 external signals + 2 internal signals
- On-chip temperature sensor
- Dual ADC conversion mode

- **16-channels Touch-Key detection timers**
- **Multiple timers**

- 4×16-bit advanced timers, support dead-zone control and emergency braking, provide PWM complementary output for motor control
- 4×16-bit general-purpose timers, provide input capture/output comparison/PWM/pulse counting/incremental encoder input
- 2 basic timers
- 2 watchdog timers (independent watchdog and window watchdog)
- SysTick: 64-bit counter

- **Communication interfaces:**

- 8 USART interfaces (including 5 UARTs)
- 2 I2C interfaces (support SMBus/PMBus)
- 3 SPI interfaces (SPI2, SPI3 for I2S2, I2S3)
- USB2.0 full-speed host/device interface, built-in PHY
- USB2.0 full-speed OTG interface
- USB2.0 high-speed host/device interface, built-in PHY
- 2 CAN interfaces (2.0B active)
- SDIO host interface (MMC, SD/SDIO, CE-ATA)
- FSMC memory interface
- Digital video port (DVP)
- Gigabit Ethernet MAC controller, 10M PHY transceiver
- 10/100M PHY transceiver (CH32V317 only)

- **Fast GPIO port**

- 80 I/O ports, mapping 16 external interrupts

- **Security features: CRC unit, 96-bit unique ID**
- **Debug mode: 2-wire serial debug interface (SDI)**
- **Package: LQFP, QFN or TSSOP**

Chapter 1 Series Product Description

CH32V series products are industrial-grade general-purpose enhanced MCU based on 32-bit RISC-V instruction set architecture, which are divided into general, connected, wireless and other categories according to functional resources. They extend each other in terms of package category, peripheral resources and quantity, pin number and device characteristics, but maintain mutual compatibility in software, function and hardware pin configuration. it provides freedom and convenience for users to carry out product iteration and rapid application in product development.

For the features of this series of products, please refer to the datasheet.

For the peripheral function description, usage and register configuration, please refer to "CH32FV2_V3RM".

The datasheets and reference manuals can be downloaded on the official website of WCH: https://wch-ic.com

Information about the RISC-V instruction set architecture can be downloaded from: https://riscv.org/

This manual is for CH32V303, CH32V305, CH32V307, CH32V317 series datasheet. Please refer to *CH32V203DS0* for V203 series and *CH32V208DS0* for V208 series.

Table 1-1-1 CH32V303/305/307/317 Series overview

High-capacity general-purpose (V303)		Connectivity (V305)		Interconnectivity (V307)	Interconnectivity (V317)
QingKe V4F					
128K Flash	256K Flash	128K Flash	256K Flash	256K Flash	256K Flash
32K SRAM	64K SRAM	32K SRAM	64K SRAM	64K SRAM	64K SRAM
2*ADC (TKey) 2*DAC ADTM 3*GPTM CRC 3*USART 2*SPI 2*I2C USBFS CAN RTC 2*WDG 4*OPA	2*ADC (TKey) 2*DAC 4*ADTM 4*GPTM 2*BCTM CRC 8*USART/UART 3*SPI (2*I2S) 2*I2C USBFS CAN RTC 2*WDG 4*OPA RNG SDIO FSMC	2*ADC (TKey) 2*DAC 4*ADTM 4*GPTM 2*BCTM CRC 5*USART/UART 3*SPI (2*I2S) 2*I2C OTG_FS USBHS (+PHY) 2*CAN RTC 2*WDG 4*OPA RNG SDIO	2*ADC (TKey) 2*DAC 4*ADTM 4*GPTM 2*BCTM CRC 5*USART/UART 3*SPI (2*I2S) 2*I2C OTG_FS USBHS (+PHY) 2*CAN RTC 2*WDG 4*OPA RNG	2*ADC (TKey) 2*DAC 4*ADTM 4*GPTM 2*BCTM CRC 8*USART/UART 3*SPI (2*I2S) 2*I2C OTG_FS USBHS (+PHY) 2*CAN RTC 2*WDG 4*OPA RNG SDIO FSMC DVP ETH-1000M MAC ETH-10M PHY	2*ADC (TKey) 2*DAC 4*ADTM 4*GPTM 2*BCTM CRC 8*USART/UART 3*SPI (2*I2S) 2*I2C OTG_FS USBHS (+PHY) 2*CAN RTC 2*WDG 4*OPA RNG SDIO DVP ETH-10M/100M PHY

Note: The number or function of some peripherals of the same type of product may be limited by the package, so please check the product package when selecting.

Table 1-1-2 CH32V203/208 Series overview

Small-and-medium capacity general-purpose (V203)		Wireless (V208)
QingKe V4B		QingKe V4C
32K Flash	64K Flash	128K Flash
10K SRAM	20K SRAM	64K SRAM
2*ADC (TKey) ADTM 3*GPTM CRC 2*USART SPI I2C USBD USBFS CAN RTC 2*WDG 2*OPA	2*ADC (TKey) ADTM 3*GPTM CRC 4*USART 2*SPI 2*I2C USBD USBFS CAN RTC 2*WDG 2*OPA	ADC (TKey) ADTM 3*GPTM GPTM (32) CRC 4*USART/UART 2*SPI 2*I2C USBD USBFS CAN RTC 2*WDG 2*OPA ETH-10M (+PHY) BLE5.3

Note: The number or function of some peripherals of the same type of product may be limited by the package, so please check the product package when selecting.

Abbreviations:

ADTM: Advanced-control timer

GPTM: General-purpose timer

GPTM (32): 32-bit General-purpose timer

BCTM: Basic timer

OPA: Operational amplifier/comparator

RNG: Random number generator

USBD: Universal serial bus full-speed device

USBFS: Universal serial bus full-speed host/device

USBHS: Universal serial bus high-speed host/device

Table 1-2 Overview of MCU Cores

Feature / Core	Instruction Set	Hardware stack level	Interrupt nesting level	Fast interrupt channels	Integer division period	Vector table mode	Extended instruction	Memory protection
QingKe V4B	IMAC	2	2	4	9	Address or instruction	Support	No
QingKe V4C	IMAC	2	2	4	5	Address or instruction	Support	Standard
QingKe V4F	IMAFC	3	8	4	5	Address or	Support	Standard

						instruction		

Note: For information about the core, please refer to "QingKeV4_Processor_Manual".

Chapter 2 Specification

CH32V30x and CH32V31x series is a 32-bit RISC-V core MCU based on QingKe V4F microprocessor. It works at 144MHz frequency and has built-in high-speed memory. Multiple buses work synchronously in the system structure, providing rich peripheral functions and enhanced Imax O ports. This series includes 2 12-bit ADC modules, 2 12-bit DAC modules, multiple timers, multi-channel touch key capacitance detection (TKey) and other functions, as well as standard and dedicated communication interfaces: I2C, I2S, SPI, USART, SDIO, CAN controller, USB2.0 full-speed host / device controller, USB2.0 high-speed host / device controller (built-in 480Mbps transceiver), digital image interface, Gigabit Ethernet controller, etc.

The rated working voltage of the product is 3.3V, and the working temperature range is -40°C～85°C in industrial grade. It supports several power-saving operating modes to meet the product's low-power application requirements. Various models in the series are different in terms of resource allocation, number of peripherals, peripheral functions, etc., and can be selected as needed.

2.1 Model Comparison

Table 2-1-1 CH32V303/305/307 products resource allocation

Part No. / Differences		CH32V303				CH32V305				CH32V307		
		CB	RB	RC	VC	FB	GB	CC	RB	RC	WC	VC
Pin count		48	64	64	100	20	28	48	64	64	68	100
Flash (bytes)		128K	128K	256K(1)	256K(1)	128K	128K	256K(1)	128K	256K(1)	256K(1)	256K(1)
SRAM (bytes)		32K	32K	64K(1)	64K(1)	32K	32K	64K(1)	32K	64K(1)	64K(1)	64K(1)
GPIO port count		37	51	51	80	17	24	41	51	51	54	80
GPIO power supply		Shared	Independent supply V_{IO}			Shared	Independent supply V_{IO}	Shared	Independent supply V_{IO}			
Timer	Advanced-control (16-bit)	1	1	4	4	4	4	4	4	4	4	4
	General-purpose (16-bit)	3	3	4	4	4	4	4	4	4	4	4
	Basic (16-bit)	-		2	2	2	2	2	2	2	2	2
	Watchdog	2 (WWDG + IWDG)										
	SysTick (64-bit)	Supported										
RTC		Supported										
ADC/TKey	Unit	2	2	2	2	2	2	2	2	2	2	2
	Channel	10	16	16	16	1	6	16	16	16	16	16

Differences \ Part No.		CH32V303				CH32V305				CH32V307		
		CB	RB	RC	VC	FB	GB	CC	RB	RC	WC	VC
DAC (Unit)		2	2	2	2	DAC2	2	2	2	2	2	2
OPA/CMP		4	4	4	4	-	OPA3	4	4	4	4	4
RNG		-	-	1	1	1	1	1	1	1	1	1
Communication interfaces	USART/UART	3	3	8	8	USART1 USART3	5	5	5	8	8	8
	SPI	2	2	3	3	SPI2	3	3	3	3	3	3
	I2S	-	-	2	2	I2S2	2	2	2	2	2	2
	I2C	2	2	2	2	2	2	2	2	2	2	2
	CAN	1	1	1	1	CAN2	1	2	2	2	2	2
	SDIO	-	-	1	1	-	1	-	1	1	1	1
	USB (FS) / USB HD	1	1	1	1	-	-	1	1	1	1	1
	USBHS (include PHY)	-				1	1	1	1	1	1	1
	Ethernet	-								1G MAC+10M PHY		
	DVP	-										1
	FSMC	-			1	-						1
CPU main frequency		Max: 144MHz										
Operating temperature		Industrial-grade: -40°C~85°C										
Package form		LQFP48	LQFP64M		LQFP100	TSSOP20	QFN28	LQFP48	LQFP64M	LQFP64M	QFN68	LQFP100

Note: 1. The products with 256K FLASH+64K SRAM support user select word to be configured as one of several combinations of (192K FLASH+128K SRAM), (224K FLASH+96K SRAM), (256K FLASH+64K SRAM), (288K FLASH+32K SRAM). On this basis, the 256K FLASH+64K SRAM product with the sixth inverted batch number not equal to 0 has also added a configuration combination: (128K FLASH+192K SRAM). FLASH flash represents the zero-waiting running area R0WAIT, and the product of 256K FLASH+64K SRAM supports the non-zero waiting area of (480K-R0WAIT) bytes.

3. The functions related to pin signals such as PWM and capture in the timer need to be combined with the pins packaged in the actual chip, and some packaged chips cannot be used without being led out.

Table 2-1-2 CH32V317 products resource allocation

Differences \ Part No.		CH32V317	
		WC	VC
Pin count		68	100
Flash (bytes)		256K(1)	256K(1)
SRAM (bytes)		64K(1)	64K(1)
GPIO port count		48	70
GPIO power supply		Independent supply V_{IO}	
Timer	Advanced-control (16-bit) (2)	4	4
	General- purpose	4	4

Differences \ Part No.			CH32V317	
			WC	VC
	(16-bit) (2)			
	Basic (16-bit)		2	2
	Watchdog		2 （ WWDG + IWDG ）	
	SysTick (64-bit)		Supported	
RTC			Supported	
ADC/TKey		Unit	2	2
		Channel	16	16
DAC (Unit)			2	2
OPA			4	4
RNG			1	1
Communication interfaces	USART/UART		8	8
	SPI		3	3
	I2S		2	2
	I2C		2	2
	CAN		2	2
	SDIO		1	1
	USB (FS)	USBHD	1	1
	USBHS (include PHY)		1	1
	Ethernet		MAC+10M/100M PHY	
	DVP		-	1
	FSMC		-	
CPU main frequency			Max: 144MHz	
Operating temperature			Industrial-grade: -40°C~85°C	
Package form			QFN68	LQFP100

Note:

1.CH32V317 supports one of several combinations of (192K FLASH+128K SRAM), (224K FLASH+96K SRAM), (256K FLASH+64K SRAM), (288K FLASH+32K SRAM) and (128K FLASH+192K SRAM). FLASH flash represents a zero-waiting running area R0WAIT, and CH32V317 supports a non-zero waiting area of (480K-R0WAIT) bytes.

2. PWM, capture and other functions related to pin signals in the timer need to be combined with the pins of the actual chip package, and some packaged chips cannot be used without being led out.

2.2 System Architecture

The microcontroller is based on the RISC-V instruction set architecture (ISA) in which the core, arbitration unit, DMA module, SRAM storage and other parts are interacted through multiple sets of buses. A general-purpose DMA controller is integrated in the chip to reduce the burden on the CPU and improve access efficiency. The application of a multi-level clock management mechanism reduces the operating power consumption of peripherals. At the same time, it has a data protection mechanism and measures such as automatic clock switching protection to increase system stability. The following figure is a block diagram of the overall internal structure of

the series of products.

Figure 2-1-1 CH32V303/305/307 System block diagram

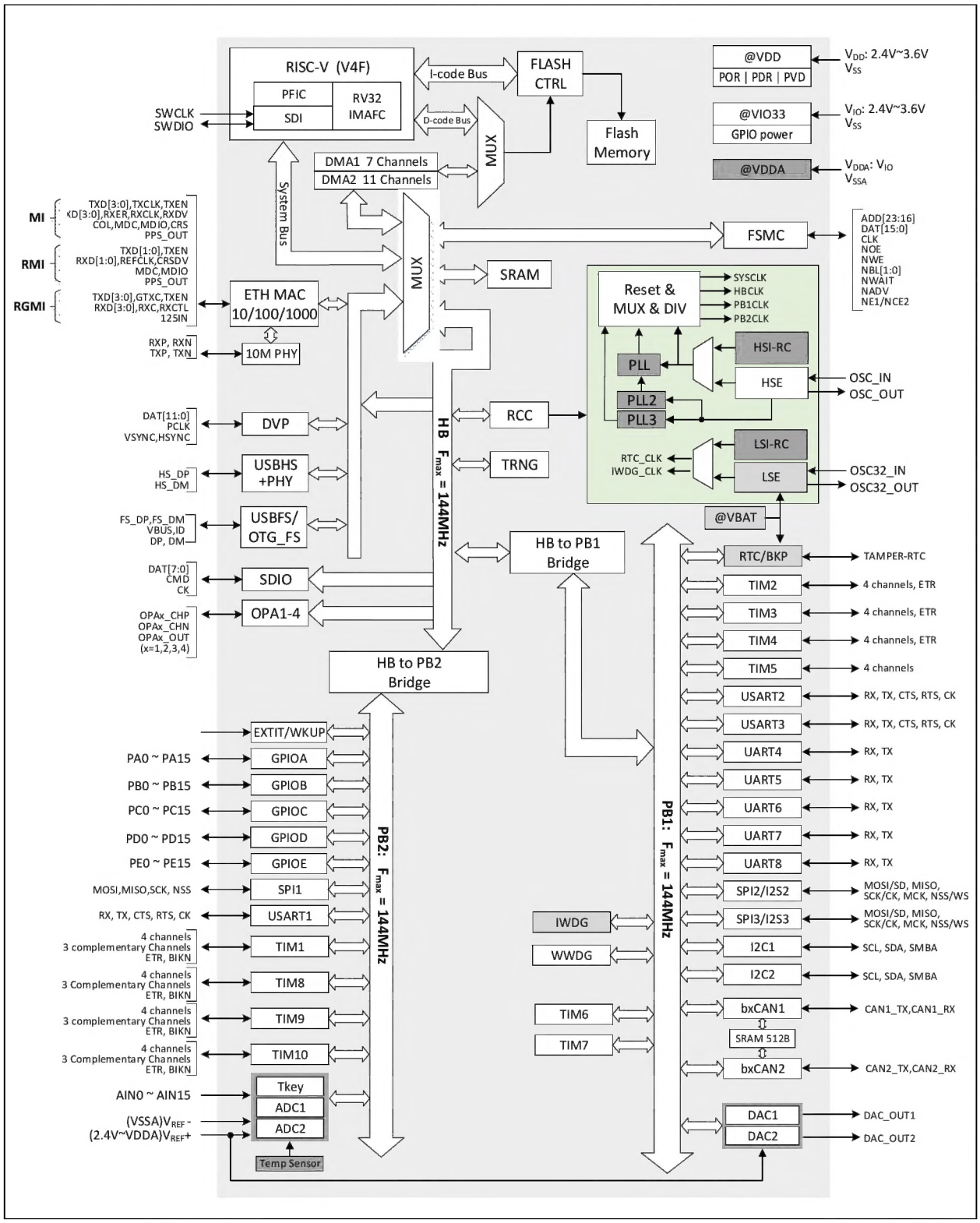
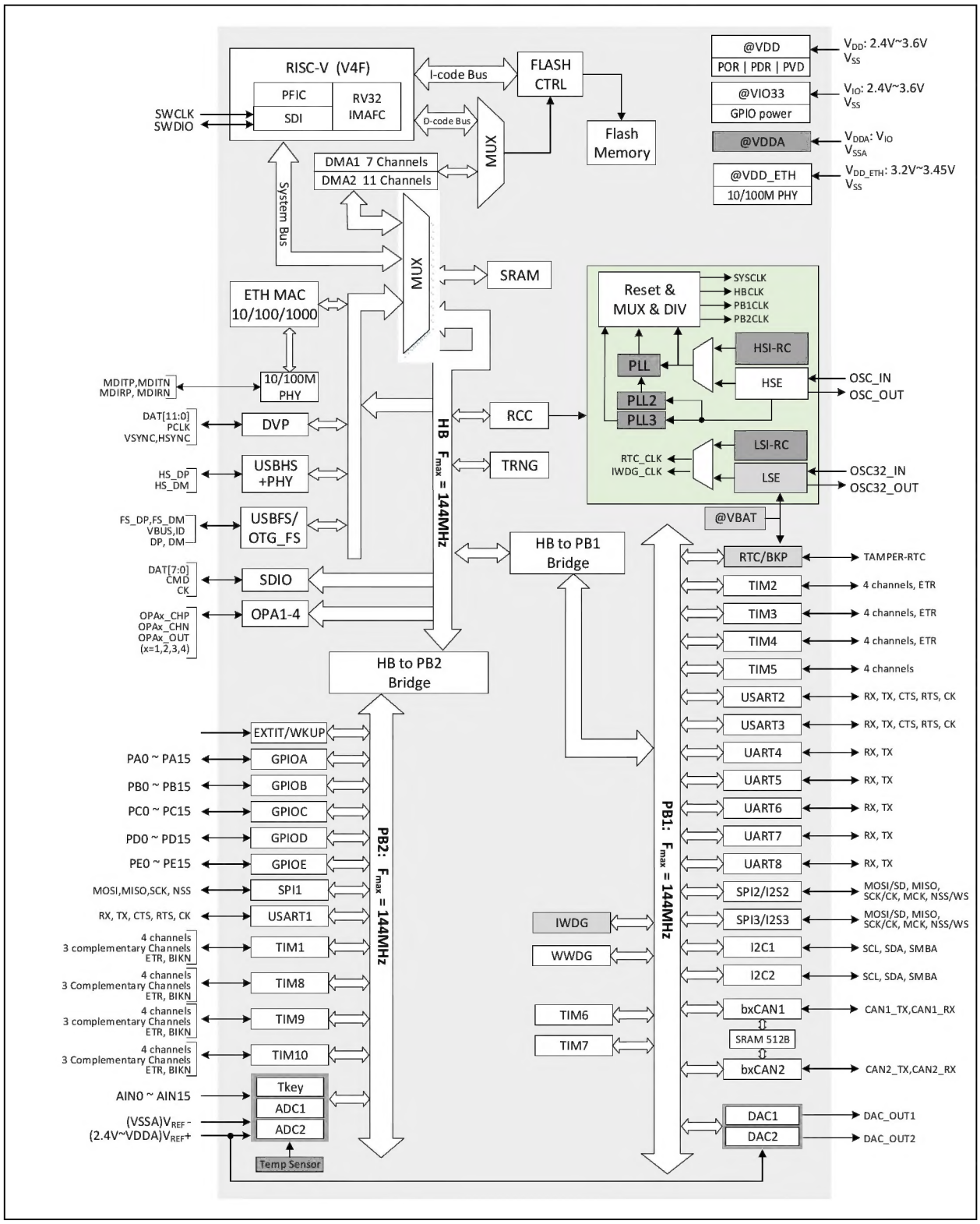
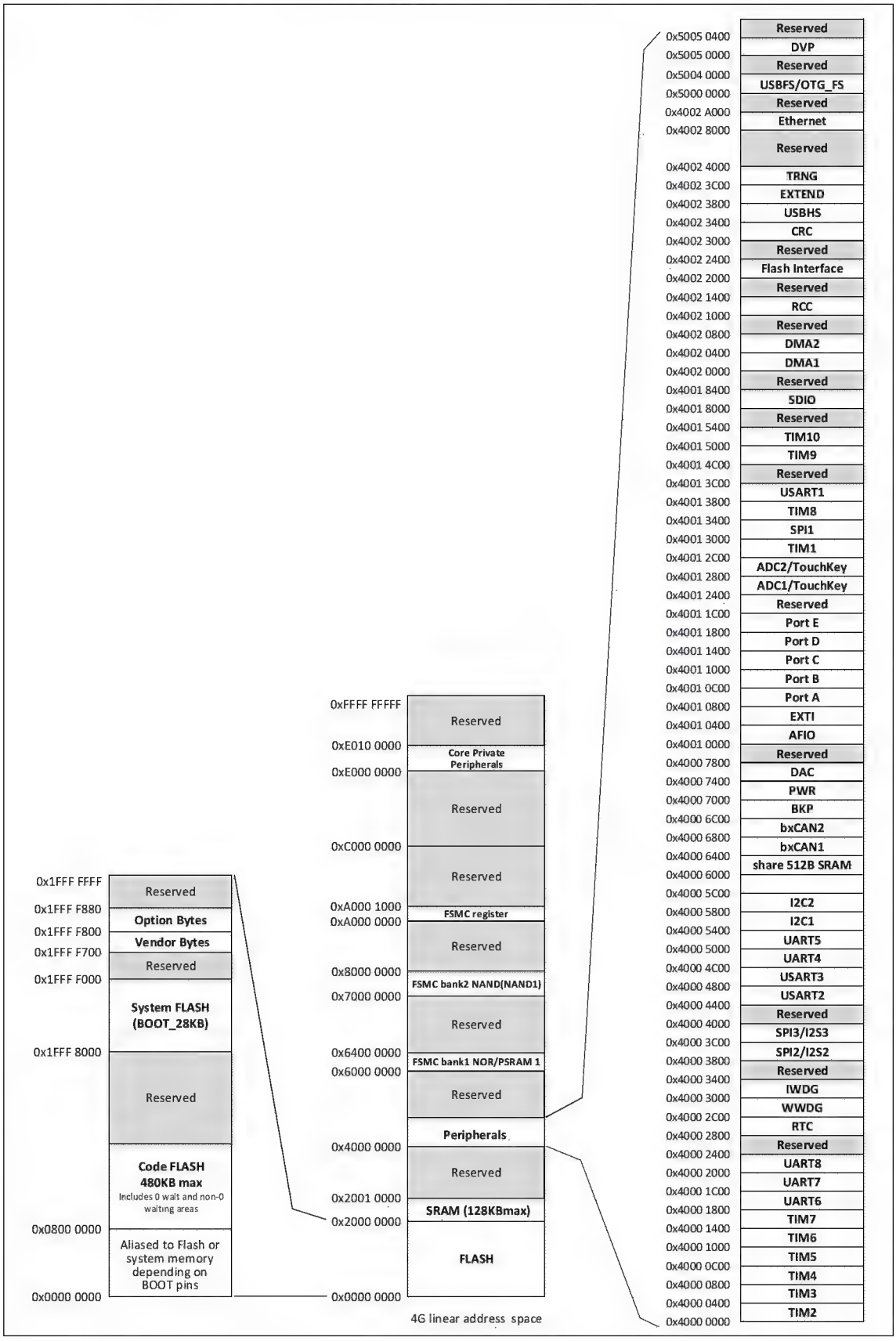


Figure 2-1-2 CH32V317 System block diagram



2.3 Memory Map

Figure 2-2 Memory address map



2.4 Clock Tree

Four groups of clock sources are introduced into the system: internal high-frequency RC oscillator (HSI), internal low-frequency RC oscillator (LSI), external high-frequency oscillator (HSE), and external low-frequency oscillator (LSE). Among them, the low-frequency clock source provides the clock reference for RTC and independent watchdog. The high-frequency clock source is directly or indirectly multiplied by the PLL and output as the system clock (SYSCLK). The system clock is then provided by each prescaler to provide the HB domain, PB1 domain, PB2 domain peripheral control clock and sampling or output clock. Some modules need to be directly provided by the PLL clock.

Figure 2-3 CH32V305/307/317 clock tree block diagram

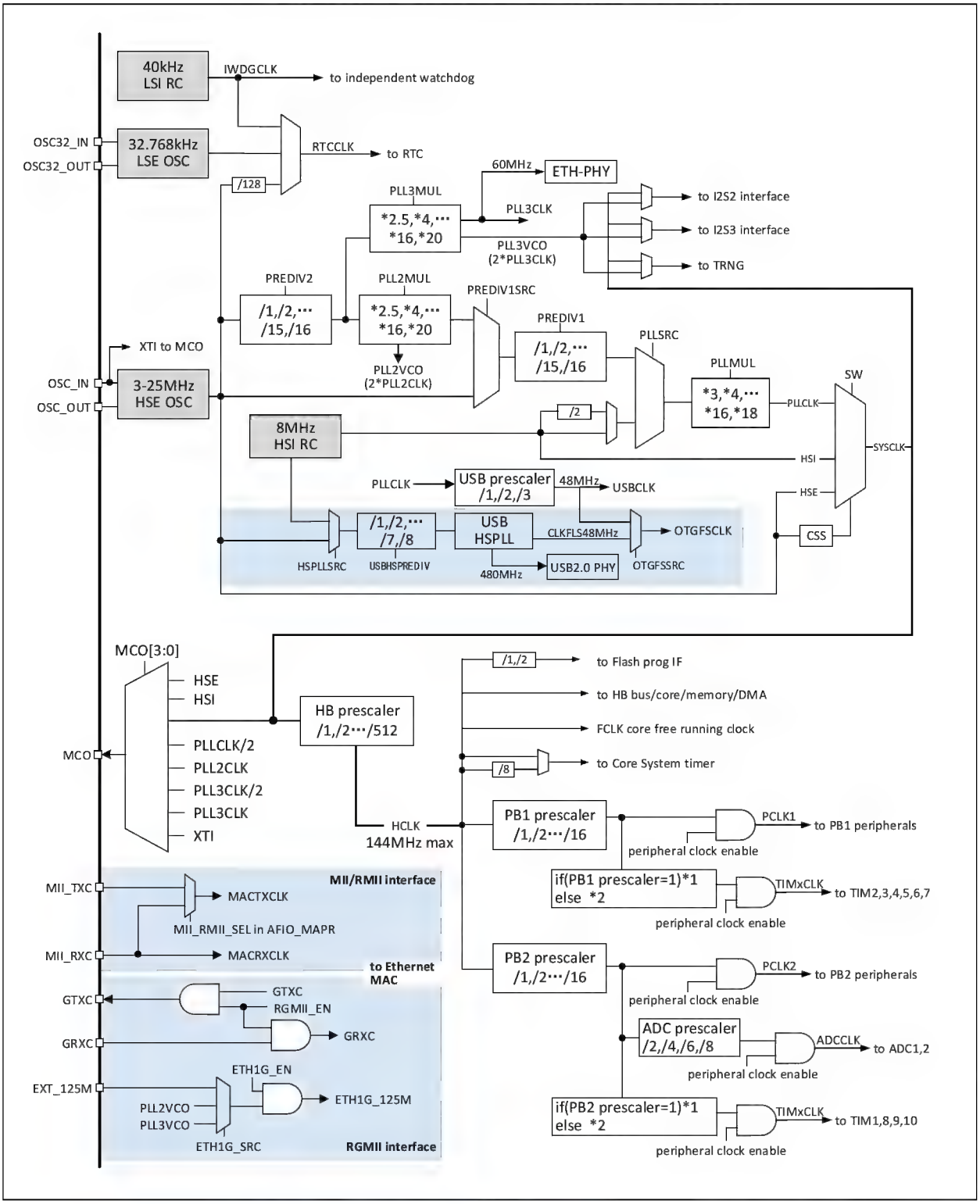
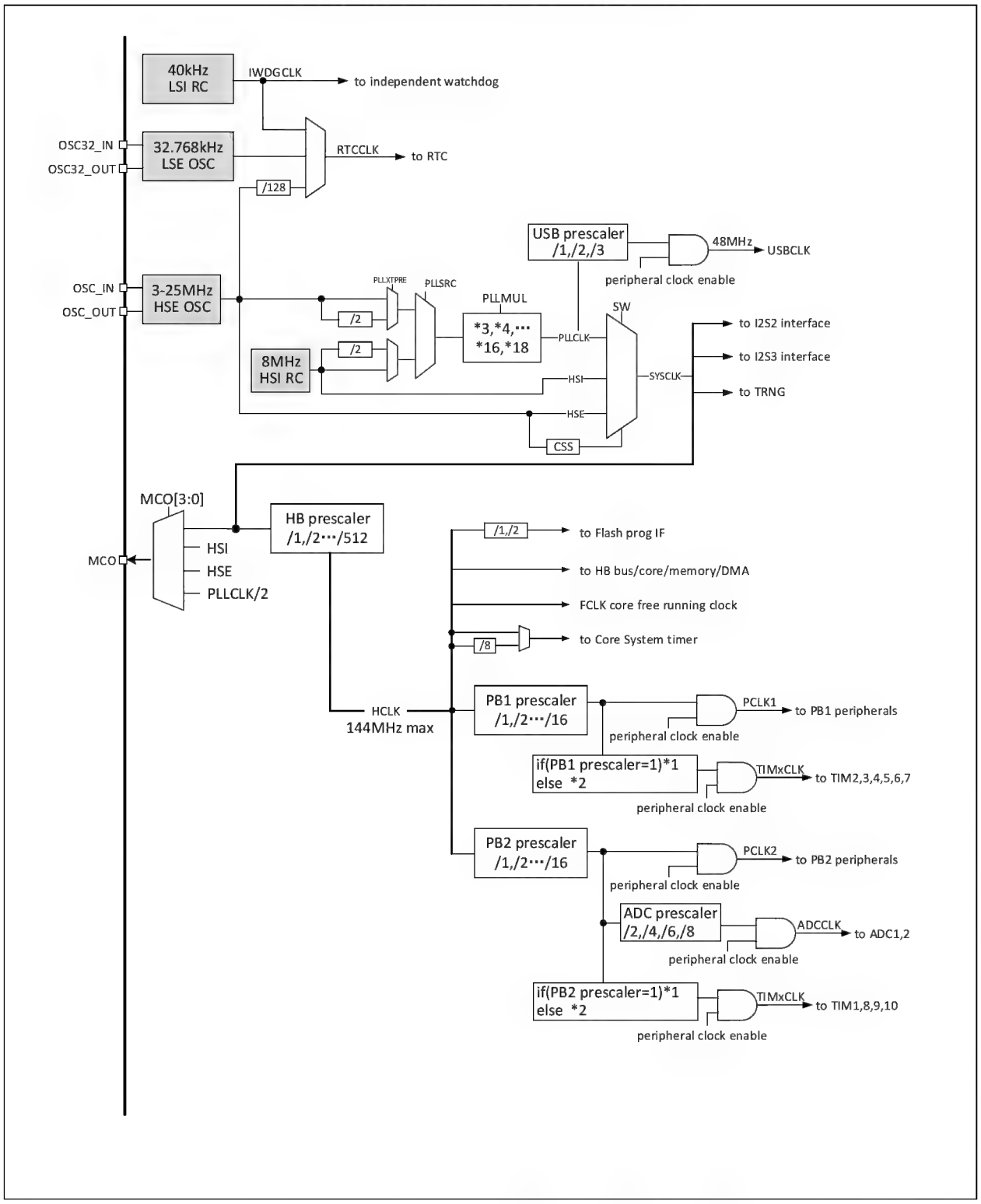


Figure 2-4 CH32V303 clock tree block diagram



Note: 1. When using USB, the CPU clock speed must be 48MHz or 96MHz or 144MHz. When system wakes up from Stop mode or Standby mode, the system will automatically select HSI as the system clock frequency.

2.5 Functional Description

2.5.1 RISC-V4F Processor

RISC-V4F supports the IMAFC subset of the RISC-V instruction set with the addition of single-precision floating-point operations. The processor is managed internally in a modular fashion and contains units such as a

fast programmable interrupt controller (PFIC), memory protection, branch prediction mode, and extended instruction support. Externally multiple buses are connected to external unit modules to enable interaction between external function modules and the core.

QingKe microprocessor can be flexibly applied in different scenarios, such as small-area low-power embedded scenarios, high-performance application operating system scenarios, etc., due to its minimal instruction set, multiple working modes, and modular customization extensions.

- Support machine and user privilege mode
- Fast Programmable Interrupt Controller (FPIC)
- Multi-level hardware interrupt stack
- 2-wire Serial debug interface
- Standard memory protection design
- Static or dynamic branch prediction, efficient jump, conflict detection
- Custom extended instructions

2.5.2 On-chip Memory and Boot Mode

Up to 128K bytes of built-in SRAM area, used to store data, data will be lost after power failure. The specific capacity depends on the corresponding chip model.

Built-in program flash memory storage area (Code FLASH) of up to 480K bytes, i.e., user area, is used for user's application program and constant data storage. It includes a zero-wait program run area and a non-zero-wait area. The specific size of the area corresponds to the chip model.

Built-in 28K bytes System FLASH, i.e., BOOT area, is used for system boot program storage (manufacturer's cured bootloader).

128 bytes for system non-volatile configuration information storage area, for the manufacturer's configuration word storage, factory-cured, the user can not be modified.

128 bytes are used for user-defined information storage area for user option byte storage.

At startup, one of 3 boot modes can be selected through the boot pins (BOOT0 and BOOT1):

- Boot from program flash
- Boot from system memory
- Boot from internal SRAM

The bootloader is stored in the system memory, and the contents of the program Flash memory storage can be reprogrammed through the USART1 and USB interface.

2.5.3 Power Supply Scheme

(1) CH32V303/305/307

- V_{DD} = 2.4[(1)]~3.6V: provides power to some of the I/O pins and internal voltage regulators, including built-in USB PHY and Ethernet PHY.
- V_{IO} = 2.4[(1)]~3.6V: It supplies power to most of the I/O pins, which determines the pin output high voltage amplitude. Normal work during operation, the V_{IO} voltage cannot be higher than the V_{DD} voltage.
- V_{DDA} = 2.4[(1)]~3.6V: It supplies power to the analog part of the high-frequency RC oscillator, ADC, temperature sensor,OPA, DAC and PLL. The V_{DDA} voltage must be the same as the V_{IO} voltage (If V_{DD} is powered down and V_{IO} is live, Then V_{DDA} must be live and consistent with V_{IO}). When using ADC, V_{DDA} must not be less than 2.4V.
- V_{BAT} = 1.8~3.6V: Optional standby power supply. When V_{DD} is turned off, (through the internal power switch) independently powers the RTC, external low-frequency oscillator and backup registers.

(2) CH32V317

- V_{DD} = 2.4(1)~3.6V: Power supply for some I/O pins and internal voltage regulators, including built-in USBPHY and Ethernet 10MPHY.
- V_{IO} = 2.4(1)~3.6V: Most I/O pins supply power, which determines the high voltage amplitude of pin output. During normal operation, the V_{IO} voltage cannot be higher than the VDD voltage.
- V_{DDA} = 2.4(1)~3.6V: Power supply for high frequency RC oscillator, ADC, temperature sensor, OPA, DAC and analog part of PLL. The voltage of V_{DDA} must be the same as that of V_{IO} (if V_{DDA} is powered off and V_{IO} is charged, V_{DDA} must be charged and consistent with V_{IO}). When using ADC, V_{DDA} shall not be less than 2.4V.
- V_{DD_ETH} = 2.4(1)~3.6V: Built-in 10/100M Ethernet PHY power supply. It is suggested to connect a capacitance of 1 UF ~ 4.7 UF to the ground, and support 10uF but need to connect 0.1uF in parallel.
- V_{DDK}: The internal power supply LDO decoupling terminal needs an external decoupling capacitor with a capacity of 1uF.
- V_{BAT} = 1.8~3.6V: Optional backup power supply, which supplies power to RTC, external low-frequency oscillator and backup register separately (through internal power switch) when V_{DD} is turned off.

2.5.4 Power Supply Monitor

The product integrates a power-on reset (POR)/power-down reset (PDR) circuit, which is always in operation. When V_{DD} is lower than the set threshold ($V_{POR/PDR}$), the device is reset without the need for an external reset circuit.

In addition, the system is equipped with a programmable voltage monitor (PVD), which needs to be turned on by software to compare the voltage of V_{DD} power supply with the set threshold V_{PVD}.

Turn on the corresponding edge interrupt of PVD, and you can receive interrupt notification when V_{DD} drops to the PVD threshold or rises to the PVD threshold. Refer to Chapter 4 for the values of $V_{POR/PDR}$ and V_{PVD}.

2.5.5 Voltage Regulator

After reset, the regulator is automatically turned on, and there are 3 operation modes according to the application mode.

- ON mode: normal operation, providing stable core power.
- Low-power mode: When the CPU enters Stop mode, the regulator can be selected to run with low- power consumption.
- OFF mode: When the CPU enters Standby mode, it automatically switches the regulator to this mode, the voltage regulator output is in high impedance, and the core power.

The voltage regulator is always ON after reset. It is OFF in Standby mode, and the regulator output is in high impedance.

2.5.6 Low-power Mode

The system supports 3 low-power modes, which can be selected for low-power consumption, short start-up time and multiple wake-up events to achieve the best balance.

- Sleep mode

In Sleep mode, only the CPU clock is stopped, but all peripheral clocks are powered normally and the peripherals are in a working state. This mode is the shallowest low-power mode, but it is the fastest mode to wake-up the system.

Exit condition: any interrupt or wake-up event.

- Stop mode

In this mode, the FLASH enters low-power mode, and the PLL, HSI RC oscillator and HSE crystal oscillator are

turned off. In the case of keeping the contents of SRAM and registers not lost, the Stop mode can achieve the lowest power consumption.

Exit conditions: any external interrupt/event (EXTI signal), external reset signal on NRST, IWDG reset, among which EXTI signal includes one of 16 external I/O ports, PVD output, RTC alarm clock, Ethernet wake-up signal or USB wake-up signal.

- Standby mode

In this mode, the main LDO of the system is turned off, the low-power LDO supplies power to the wake-up circuit, all other digital circuits are powered off, and the FLASH is powered off. The system wakes up from Standby mode will generate a reset, and SBF (PWR_CSR) will be set at the same time. After waking up, check the SBF status to know the low-power mode before waking up. SBF is cleared by the CSBF (PWR_CR) bit. In the Standby mode, the contents of 32KB of SRAM can be kept (depending on the planning and configuration before going to bed), and the contents of the backup registers are kept.

Exit conditions: any external interrupt/event (EXTI signal), external reset signal on NRST, IWDG reset, a rising edge on the WKUP pin, where EXTI signal includes one of 16 external I/O ports, RTC alarm clock, Ethernet Wake-up signal, USB.

2.5.7 CRC (Cyclic Redundancy Check) Calculation Unit

The CRC (cyclic redundancy check) calculation unit uses a fixed polynomial generator to generate a CRC code from a 32-bit data word. In many applications, CRC-based technology is used to verify the consistency of data transmission or storage. Within the scope of the EN/IEC 60335-1 standard, a means of detecting flash errors is provided. The CRC calculation unit can be used to calculate the signature of the software in real time and compare it with the signature generated when the software is linked and generated.

2.5.8 Fast Programmable Interrupt Controller (FPIC)

The product has a built-in Fast Programmable Interrupt Controller (FPIC), which supports up to 255 interrupt vectors, and provides flexible interrupt management functions with minimal interrupt latency. The current product manages 8 core private interrupts and 88 peripheral interrupt management, and other interrupt sources are reserved. FPIC registers can be accessed in user and machine privileged modes.

- 2 individual maskable interrupts
- A non-maskable interrupt NMI
- Support hardware interrupt stack (HPE) without instruction overhead
- 4-channel vector table free interrupts (VTF)
- Vector table supports address or command mode
- Configurable interrupt nesting depth, up to 8 levels
- Support interrupt tail-chaining

2.5.9 External Interrupt/Event Controller (EXTI)

The external interrupt/event controller contains a total of 19 edge detectors for generating interrupt/event requests. Each interrupt line can independently configure its trigger event (rising edge or falling edge or both edges), and can be individually masked; the suspend register maintains all interrupt request states. EXTI can detect that the pulse width is smaller than the clock period of the internal PB2. Up to 80 general-purpose I/O ports can be connected to 16 external interrupt lines.

2.5.10 General DMA Controller

The system has built-in 2 groups of general-purpose DMA controllers, manages 18 channels in total, and flexibly handles high-speed data transmission from memory to memory, peripherals to memory, and memory to

peripherals, and supports ring buffer mode. Each channel has a dedicated hardware DMA request logic to support one or more peripherals' access requests to the memory. The access priority, transfer length, source address and destination address of the transfer can be configured.

The main peripherals used by DMA include: general/advanced/basic timers TIMx, ADC, DAC, I²S, USART, I²C, SPI, and SDIO.

Note: DMA1, DMA2 and CPU access the system SRAM after arbitration by the arbiter.

2.5.11 Clock and Boot

The system clock source HSI is turned on by default. After the clock is not configured or reset, the internal 8MHz RC oscillator is used as the default CPU clock, and then an external 3～25MHz clock or PLL clock can be additionally selected. When the clock security mode is turned on, if the HSE is used as the system clock (directly or indirectly), the system clock will automatically switch to the internal RC oscillator when the external clock is detected to be invalid, and the HSE and PLL will be automatically turned off at the same time; in low-power consumption mode, the system will automatically switch to the internal RC oscillator after waking up. If the clock interrupt is enabled, the software can receive the corresponding interrupt.

Multiple prescalers are used to configure the frequency of HB. The high-speed PB (PB2) and low-speed PB (PB1) regions provide peripheral clocks with a maximum frequency of 144MHz. Refer to the clock tree block diagram in Figure 2-3. The clock source of the I2S unit is another dedicated PLL (PLL3), so that the I²S master clock can generate all standard sampling frequencies between 8kHz and 192kHz.

2.5.12 Real Time Clock (RTC) and Backup Registers

The RTC and the backup register are in the backup power supply area inside the system. When V_{DD} is valid, it is powered by V_{DD}, and when V_{DD} is invalid, the internal power is automatically switched to the V_{BAT} pin.

The RTC real-time clock is a set of 32-bit programmable counters, and the time base supports 20-bit prescaler for measurement in a longer period of time. The clock reference source is a high-speed external clock divided by 128 (HSE/128), external crystal low-frequency oscillator (LSE) or internal low-power RC oscillator (LSI). The LSE also has a backup power supply area, so when the LSE is selected as the RTC time base, the RTC setting and time can remain unchanged after the system resets or wakes up from Standby mode.

The backup register contains up to 42 16-bit registers, which can be used to store 84 bytes of user application data. This data can continue to be maintained after wake-up from Standby, or system Reset or power Reset. When the intrusion detection function is turned on, once the intrusion detection signal is valid, all contents in the backup register will be cleared.

2.5.13 Analog-to-digital Converter (ADC) and Touch Key Capacitance Detection (TKey)

The product has built-in 2 12-bit analog/digital converters (ADC), sharing up to 16 external channels and 2 internal channels for sampling. The programmable channel sampling time can realize single, continuous, scanning or discontinuous conversion. And supports dual ADC conversion mode. The analog watchdog function is provided to allow very precise monitoring of one or more selected channels for monitoring the signal voltage of the channel. It supports external event-triggered conversion, the trigger source includes the internal signal and external pin of the on-chip timer; it also supports the use of DMA operations.

ADC internal channel sampling includes 1 channel of built-in temperature sensor sampling and 1 channel of internal reference power sampling. The temperature sensor generates a voltage that varies linearly with temperature. The temperature sensor is internally connected to the IN16 input channel, which is used to convert

the output of the sensor to a digital value.

The touch button capacitance detection unit provides up to 16 detection channels and reuses the external channels of the ADC module. The test results are converted into output results by the ADC module, and the touch button state is identified by software calculation.

2.5.14 Digital-to-analog Converter (DAC)

The product has 2 built-in 12-bit voltage output digital / analog converters (DAC), which converts 2 digital signals into 2 analog voltage signals and outputs. It supports dual DAC channels independent or synchronous conversion, and supports external event trigger conversion. The trigger source includes the internal signal of the on-chip timer and the external pin (EXTI line 9). Triangular wave and noise generation can be realized. Support the use of DMA operations.

2.5.15 Timer and Watchdog

The timers in the system include advanced timers, general timers, basic timers, watchdog timers, and system time base timers. The number of timers included in different products in the series is different, please refer to Table 2-2 for details.

Table 2-2 Timer comparison

Timer		Resolution	Count Type	Time Base	DMA	Function
Advanced control timer	TIM1 TIM8 TIM9 TIM10	16 bits	Up Down Up/down	PB2 time domain 16-bit divider	Supported	PWM complementary output, single pulse output Input capture Output compare Timer count
General-purpose timer	TIM2 TIM3 TIM4 TIM5	16 bits	Up Down Up/down	PB1 time domain 16-bit divider	Supported	Input capture Output compare Timer count
Basic timer	TIM6 TIM7	16 bits	Up	PB1 time domain 16-bit divider	Supported	Timing count
Window watchdog		7 bits	Down	PB1 time domain 4 types of frequency division	Not supported	Timing Reset the system (normal work)
Independent watchdog		12 bits	Down	PB1 time domain 7 types of frequency division	Not supported	Timing Reset the system (normal work + low-power work)
SysTick timer		64 bits	Up/down	SYSCLK or SYSCLK/8	Not supported	Timing

- Advanced-control timer

The advanced control timer is a 16-bit auto-loading up/down counter with a 16-bit programmable prescaler. In addition to the complete general-purpose timer function, it can be regarded as a three-phase PWM generator distributed to 6 channels, with a complementary PWM output function with dead zone insertion, allowing the timer to be updated after a specified number of counter cycles to repeat counting cycle, braking function, etc. Many functions of the advanced control timer are the same as the general timer, and the internal structure is also the same. Therefore, the advanced control timer can cooperate with other TIM timers through the timer link function to provide synchronization or event link functions.

- General-purpose timer

The general timer is a 16-bit auto-loading up/down counter with a programmable 16-bit prescaler and 4 independent channels. Each channel supports input capture, output comparison, and PWM generation and single pulse mode output. It can also work with advanced control timers through the timer link function to provide synchronization or event link functions. In Debug mode, the counter can be frozen while the PWM outputs are disabled, thereby cutting off the switches controlled by these outputs. Any general-purpose timer can be used to generate PWM output. Each timer has an independent DMA request mechanism. These timers can also process signals from incremental encoders, as well as digital outputs from 1 to 3 Hall sensors.

- Basic timer

The basic timer is a 16-bit auto-load counter that supports a 16-bit programmable prescaler. Digital-to-analog conversion (DAC) can provide a clock and trigger the synchronization circuit of the DAC. The basic timers are independent of each other and do not share any resources with each other.

- Independent watchdog

The independent watchdog is a configurable 12-bit down counter that supports 7 frequency division factors. The clock is provided by an internal independent about 40kHz RC oscillator (LSI); because the LSI is independent of the main clock, it can run in Stop and Standby modes. IWDG is outside the main program and can work completely independently. Therefore, it is used to reset the entire system when a problem occurs, or as a free timer to provide timeout management for the application. It can be configured as software or hardware to start the watchdog through the option byte. In Debug mode, the counter can be frozen.

- Window watchdog

The window watchdog is a 7-bit down counter and can be set to free-running. It can be used to reset the entire system when a problem occurs. It is driven by the main clock and has an early warning interrupt function; in Debug mode, the counter can be frozen.

- SysTick timer

QingKe microprocessor core comes with a 64-bit optional increasing or decreasing counter, which is used to generate SYSTICK exceptions (exception number: 15). It can be specially used in real-time operating systems to provide "heartbeat" rhythm for the system, and can also be used as a standard 64-bit counter. It has automatic reload function and programmable clock source.

2.5.16 Universal Synchronous/Asynchronous Receiver Transmitter (USART)

The product provides 3 groups of Universal Synchronous/Asynchronous Receiver Transmitters (USART1, USART2, USART3), and 5 groups of Universal Asynchronous Receiver Transmitters (UART4, UART5, UART6, UART7, UART8). It supports full-duplex asynchronous communication, synchronous one-way communication and half-duplex single-wire communication. It also supports LIN (Local Interconnect Network), compatible with

ISO7816 smart card protocol and IrDA SIR ENDEC transmission codec specification, and modem (CTS/RTS hardware flow control) operation. It also allows multi-processor communication. It uses a fractional baud rate generator system and supports DMA operation continuous communication.

2.5.17 Serial Peripheral Interface (SPI)

Up to 3 groups of serial peripherals interface (SPI) provide master or slave operation, dynamic switching. Support multi-master mode, full-duplex or half-duplex synchronous transmission, support basic SD card and MMC mode. Programmable clock polarity and phase, data bit width provides 8 or 16-bit selection, hardware CRC generation/check for reliable communication, and continuous communication support for DMA operation.

2.5.18 I2S (audio) Interface

Up to 2 sets of standard I2S interfaces (multiplexed with SPI2 and SPI3) operate in master or slave mode. The software can be configured to transmit frames with 16/32-bit packets, support audio sampling frequencies from 8kHz to 562.2kHz, and support four audio standards. In main mode, the master clock can be output to external DAC or CODEC (decoder) at a fixed audio sampling frequency of 256x, and DMA is supported.

2.5.19 I2C Bus

Up to 2 I2C bus interfaces can work in multi-master mode or Slave mode, perform all I2C Bus specific timing, protocol, arbitration, etc. It supports both standard and fast speed, and is compatible with SMBus2.0.

The I2C interface provides 7-bit or 10-bit addressing, and supports dual slave addressing in 7-bit Slave mode. It integrates built-in hardware CRC generator/checker. It also supports DMA operation and supports SMBus bus version 2.0 / PMBus bus.

2.5.20 Controller Area Network (CAN)

The CAN interface is compatible with specifications 2.0A and 2.0B (active), the baud rate is up to 1Mbits/s, and it supports time-triggered communication functions. It can receive and send standard frames with 11-bit identifiers, as well as extended frames with 29-bit identifiers. It has 3 sending mailboxes and 2 3-level deep receiving FIFOs. Products with 2 CAN controllers share 28 configurable filters and 512 bytes of SRAM memory resources.

With 1 set of CAN controller products, there are only 14 configurable filters, and share a dedicated 512-byte SRAM memory with the USBD module for data transmission and reception. When USBD and CAN are used at the same time, in order to prevent access to SRAM conflicts, USBD can only use the lower 384 bytes.

2.5.21 Universal Serial Bus USB2.0 Full-speed Host/Device Controller (USBFS/OTG_FS)

USB2.0 full-speed host controller and device controller (USBFS) follow the USB2.0 full-speed standard. It provides 16 configurable USB device endpoints and a set of host endpoints. Support control/batch/synchronization/interrupt transmission, double buffer mechanism, USB bus suspend/resume operation, and provide standby/wake-up functions. The 48MHz clock dedicated to the USBFS module is directly generated by the internal main PLL frequency division (the PLL must be 144MHz or 96MHz or 48MHz).

OTG_FS is a dual role USB controller that supports both host-side and device-side functionality and is compatible with the On-The-Go Supplement to the USB2.0 specification. The controller can also be configured as a host-side only or device-side only controller, compatible with the USB2.0 Full Speed specification. The controller uses a 48MHz clock derived from PLL divider and key features include

- Support the USB On-The-Go Supplement (physical layer of the OTG_FS controller), defined as an optional OTG protocol in the Revision 1.3 specification
- Software configurable USB full speed host, USB full speed/low speed device, USB dual role device
- Provide power saving function

- Support control transfer, bulk transfer, interrupt transfer, real-time/synchronous transfer
- Provide bus reset, suspend, wakeup and resume functions

2.5.22 Universal Serial Bus USB2.0 High-speed Host/Device Controller (USBHS)

USB2.0 high-speed controller has dual roles of host controller and device controller, and has built-in USB-PHY physical layer transceiver of 480Mbps. When used as a host controller, it can support low-speed, full-speed and high-speed USB devices. When used as a device controller, it can be flexibly set to low-speed, full-speed or high-speed mode to adapt to a variety of applications. Key features include:

- Support USB 2.0, USB 1.1, USB 1.0 protocol specifications
- Support control transfer, bulk transfer, interrupt transfer, real-time/synchronous transfer
- Provide bus reset, suspend, wakeup and resume functions
- Support high-speed HUB
- Provide 16 groups of up and down transmission channels in device mode, supports configuration of 16 endpoint numbers
- All endpoints except device endpoint 0 support packets up to 1024 bytes, with double buffering available

2.5.23 Digital Video Port (DVP)

Digital Video Port (DVP) is used to connect to the camera module to obtain the image data stream. It provides 8/10/12bit parallel interface way of communication. It supports image data organized in original line and frame formats, such as YUV, RGB, etc., and also supports compressed image data streams such as JPEG format. When receiving, it mainly relies on VSYNC and HSYNC signal synchronization. Support image cropping function.

2.5.24 SDIO Host Controller

The SDIO host interface provides interfaces for the operation of multimedia cards (MMC), SD memory cards, SDIO cards, and CE-ATA devices. Three different data bus modes are supported: 1-bit (default), 4-bit and 8-bit. In 8-bit mode, the interface enables data transfer rates up to 48 MHz. currently the interface is fully compatible with the Multimedia Card System Specification 4.2 (forward compatible), SD I/O Card Specification 2.0, SD Memory Card Specification 2.0, and CE-ATA Digital Protocol Specification 1.1.

2.5.25 Flexible Static Memory Controller

The FSMC interface provides mainly synchronous or asynchronous memory interfaces, supporting SRAM, PSRAM, NOR and NAND devices. The internal HB transfer signal is converted to a suitable external communication protocol, allowing continuous access to 8/16/32 bit data. The sampling delay time is flexibly configurable to suit different device timings.

In addition, the FSMC can also be used to interface with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 models, making it easy to build simple graphic application environments or high-performance solutions for dedicated accelerated controllers.

2.5.26 Gigabit Ethernet controller (MAC+PHY)

The product provides an IEEE802.3-2002 compliant Gigabit Ethernet controller (MAC), which acts as the data link layer. Its Link rate supports 1Gbps at the highest speed, supports gigabit and 100 megabit and speed adaptation, and provides a MII/RMII/RGMII interface to connect to external PHY chips (such as 100Mbps's industrial physical layer chip CH182). In application, combined with TCP/IP protocol stack to achieve the development of network products.

CH32V307 chip has built-in 10Mbps Ethernet PHY physical layer transceiver; The CH32V317 chip has a built-in 10Mbps/100Mbps Ethernet PHY physical layer transceiver. Ethernet communication can be realized on a

single chip.

Key features include:

- Compliant with IEEE 802.3 protocol specification and design
- Provide RGMII, RMII, MII interfaces to external Ethernet PHY transceivers
- Support full-duplex operation and 10/100/1000Mbps data transfer rates
- Hardware automatic IPv4 and IPv6 packet integrity checks, IP/ICMP/UDP/TCP packet checks and computer frame length padding
- Multiple MAC address filtering modes
- External PHY can be configured and managed by SMI
- The application of CH32V307 chip can choose Ethernet controller MAC+built-in 10Mbps PHY or external 1Gbps PHY.
- The chip application of CH32V317 can be built-in 10Mbps/100Mbps PHY for Ethernet controller MAC+.

2.5.27 General-purpose Input and Output (GPIO)

The system provides 5 groups of GPIO ports with a total of 80 GPIO pins. Each pin can be configured by software as output (push-pull or open-drain), input (with or without pull-up or pull-down) or multiplexed peripheral function port. Most GPIO pins are shared with digital or analog multiplexed peripherals. Except for ports with analog input functions, all GPIO pins have high current passing capabilities. A locking mechanism is provided to freeze the IO configuration to avoid accidental writing to the I/O register.

Most of the IO pins in the system are provided by V_{IO}. Changing the V_{IO} power supply will change the high value of the IO pin output level to adapt to the external communication interface level. Please refer to the pin description for specific pins.

2.5.28 Random Number Generator (RNG)

The product has built-in a random number generator, which provides a 32-bit random number through the internal analog circuit.

2.5.29 Operational Amplifier/Comparator (OPA)

The product has 4 sets of operational amplifiers, which can also be used for comparators. The internal selection is associated with ADC and TIMx peripherals, whose inputs and outputs can be selected for multiple channels by changing the configuration. Support the external analog small signal to be amplified into ADC to achieve small signal ADC conversion, can also complete the signal comparator function, the comparison results are output by GPIO or directly connected to the input channel of TIMx.

2.5.30 2-wire SDI Serial Debug Interface

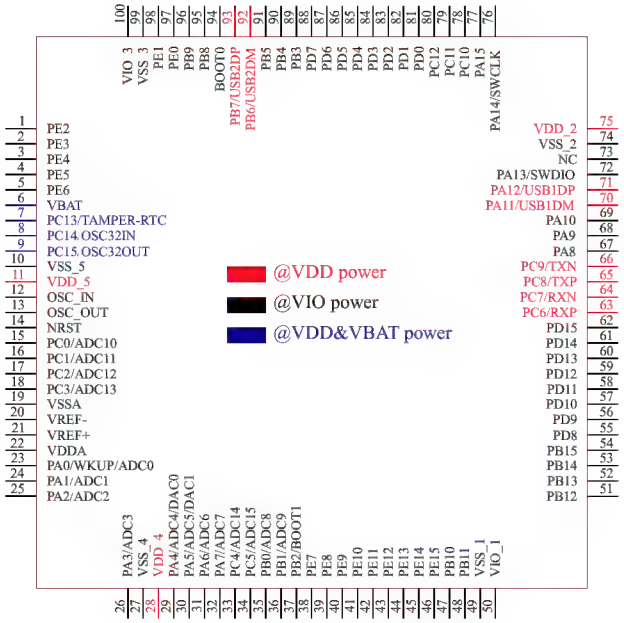
The core comes with a 2-wire serial debug interface (SDI), including SWDIO and SWCLK pins. The default debug interface pin function is turned on after the system is powered on or reset, and the SDI can be turned off according to the need after the main program is running.

Chapter 3 Pinouts and Pin Definition

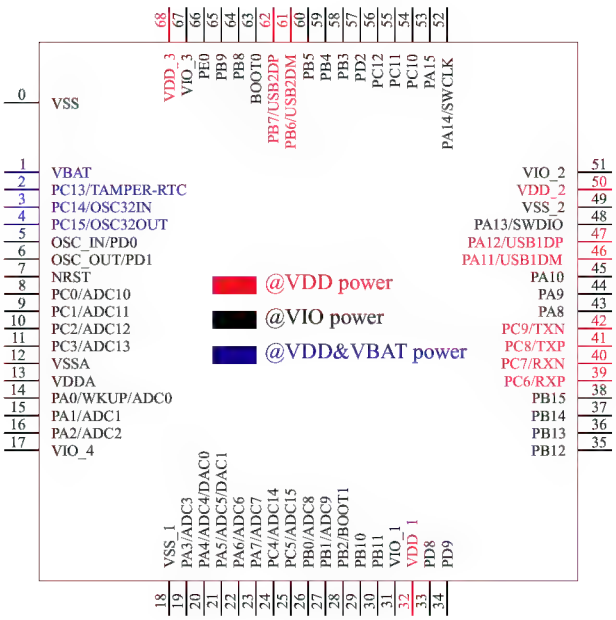
3.1 Pinouts

3.1.1 Interconnectivity Device V307

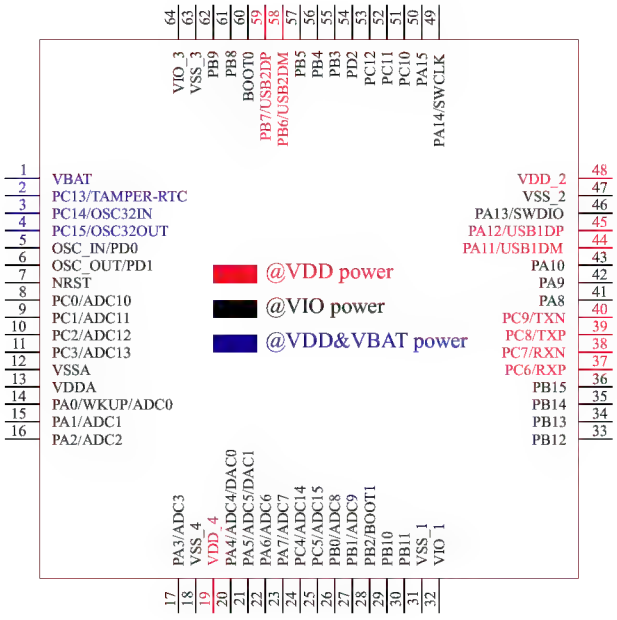
CH32V307VCT6



CH32V307WCU6

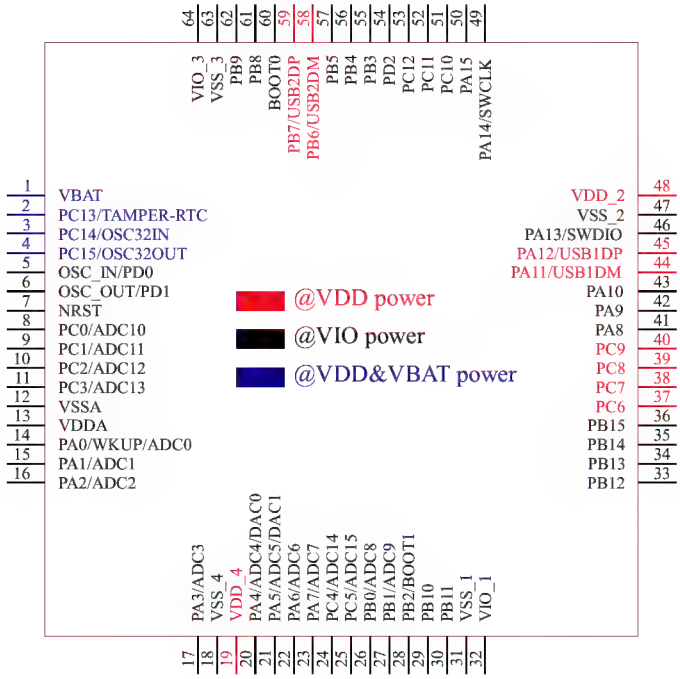


CH32V307RCT6

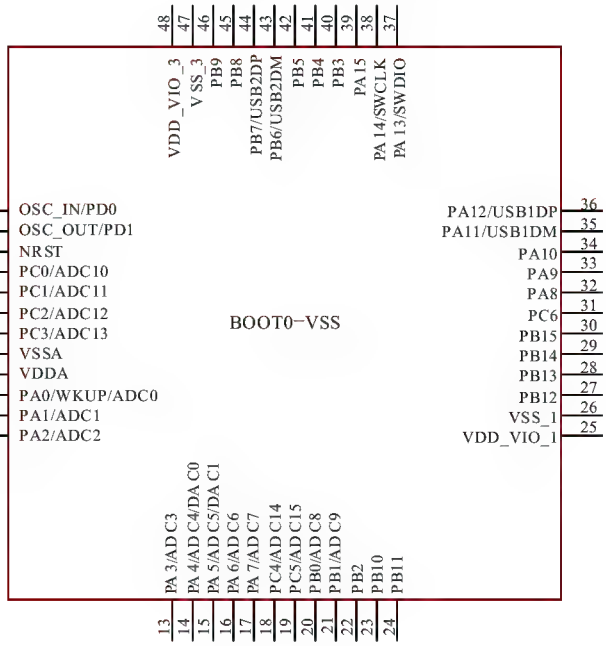


3.1.2 Connectivity Device V305

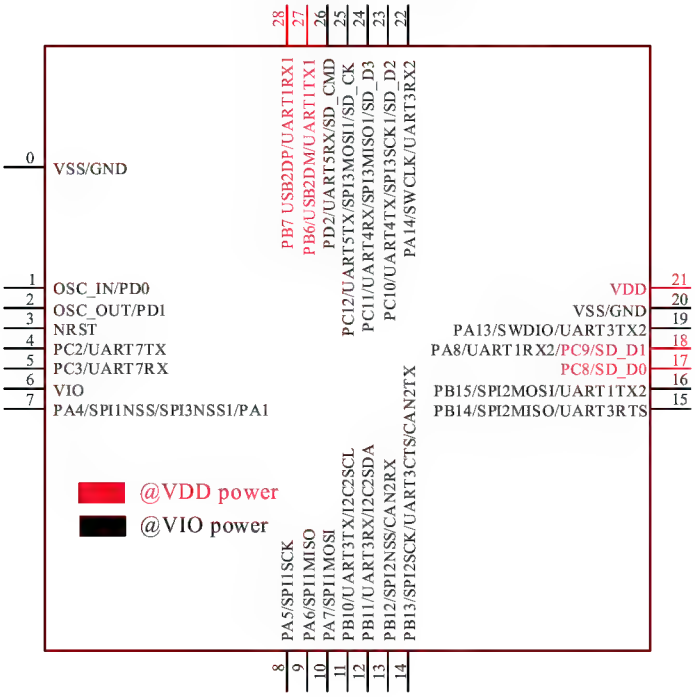
CH32V305RBT6



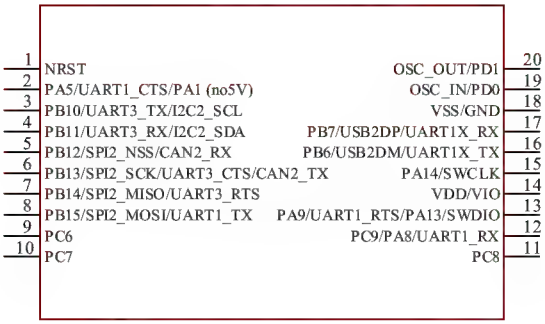
CH32V305CCT6



CH32V305GBU6

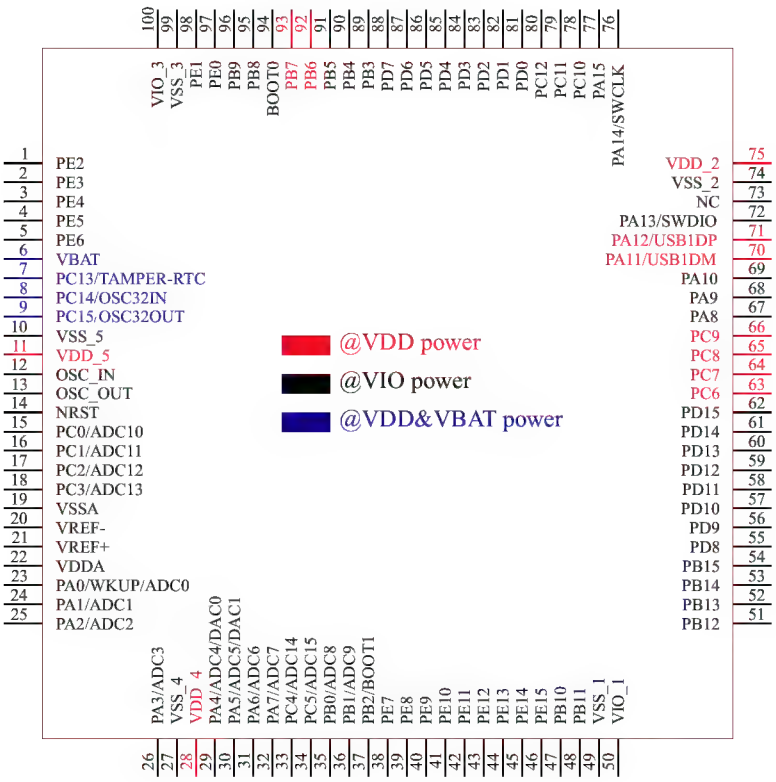


CH32V305FBP6

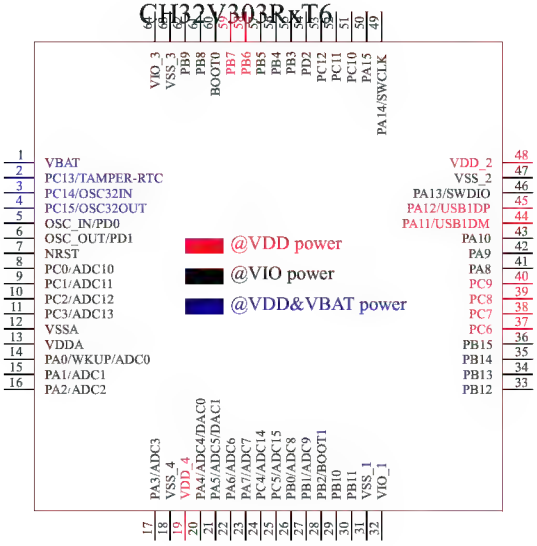


3.1.3 High-capacity General-purpose Device V303

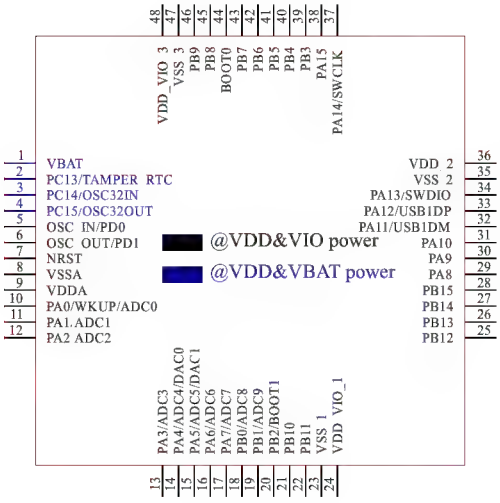
CH32V303VCT6



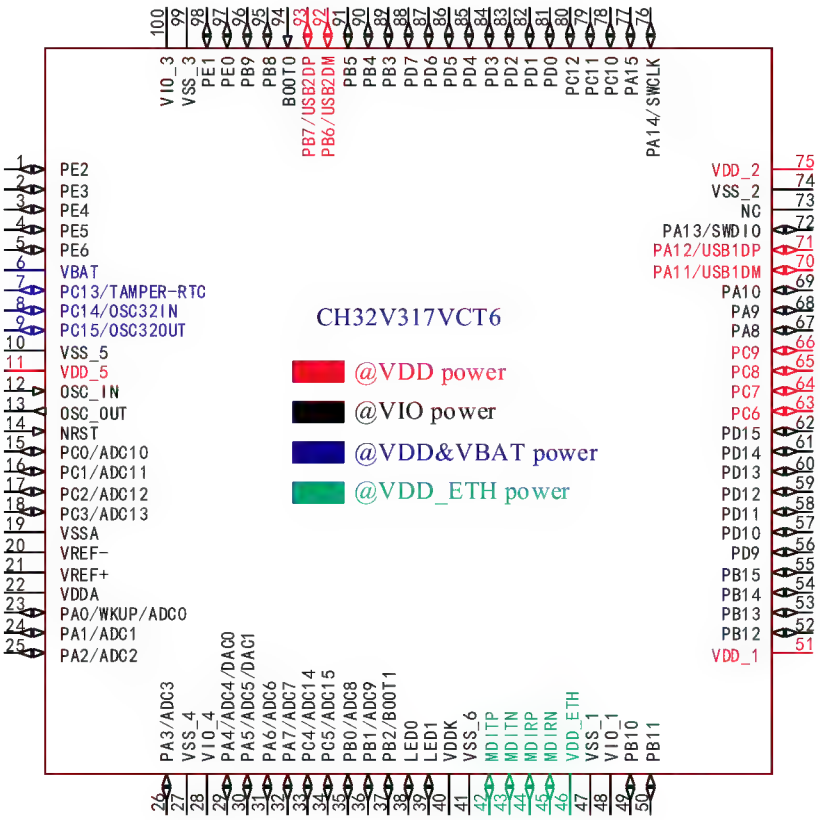
CH32V303RxT6

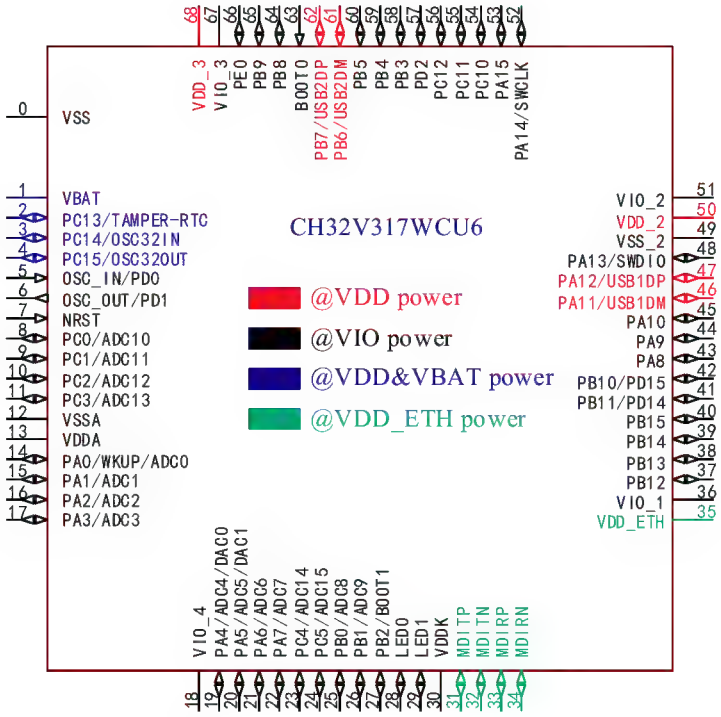


CH32V303CBT6



3.1.4 Interconnectivity Device V317





3.2 Pin Definitions

Note: The pin function in the table below refer to all functions and does not involve specific model(s). There are differences in peripheral resources between different models. Please confirm whether this function is available according to the particular model's resource table before viewing this table.

Table 3-1 CH32V303/305/307 pin definitions

Pin No.							Pin name	Pin type[1]	I/O level	Main function (after reset)	Default alternate function	Remapping function[13]
TSSOP20	QFN28	LQFP48(V305CCT	LQFP48(V303CBT	LQFP64M	QFN68	LQFP100						
18	0 20	-	-	-	0	-	VSS	P	-	VSS	-	-
-	-	-	-	-	-	1	PE2	I/O	FT	PE2	FSMC_A23	TIM10_BKIN_2 TIM10_BKIN_3
-	-	-	-	-	-	2	PE3	I/O	FT	PE3	FSMC_A19	TIM10_CH1N_2 TIM10_CH1N_3
-	-	-	-	-	-	3	PE4	I/O	FT	PE4	FSMC_A20	TIM10_CH2N_2 TIM10_CH2N_3
-	-	-	-	-	-	4	PE5	I/O	FT	PE5	FSMC_A21	TIM10_CH3N_2 TIM10_CH3N_3
-	-	-	-	-	-	5	PE6	I/O	FT	PE6	FSMC_A22	
-	-	-	1	1	1	6	V_{BAT}	P	-	V_{BAT}		
-	-	-	2	2	2	7	PC13-TAMPER-RTC[2]	I/O	-	PC13[3]	TAMPER-RTC	TIM8_CH4_1
-	-	-	3	3	3	8	PC14-OSC32_IN[2]	I/O/A	-	PC14[3]	OSC32_IN	TIM9_CH4_1
-	-	-	4	4	4	9	PC15-OSC32_OUT[2]	I/O/A	-	PC15[3]	OSC32_OUT	TIM10_CH4_1
-	-	-	-	-	-	10	V_{SS_5}	P	-	V_{SS_5}		
-	-	-	-	-	-	11	V_{DD_5}	P	-	V_{DD_5}		
19	1	1	5	5	5	12	OSC_IN	I/A	-	OSC_IN		PD0[4]
20	2	2	6	6	6	13	OSC_OUT	O/A	-	OSC_OUT		PD1[4]
1	3	3	7	7	7	14	NRST	I	-	NRST		
-	-	4	-	8	8	15	PC0	I/O/A	-	PC0	ADC_IN10 TIM9_CH1N UART6_TX ETH_RGMII_RXC	
-	-	5	-	9	9	16	PC1	I/O/A	-	PC1	ADC_IN11	

Pin No.							Pin name	Pin type(1)	I/O level	Main function (after reset)	Default alternate function	Remapping function(13)
TSSOP20	QFN28	LQFP48(V305CCT	LQFP48(V303CBT	LQFP64M	QFN68	LQFP100						
											TIM9_CH2N UART6_RX ETH_MII_MDC ETH_RMII_MDC ETH_RGMII_RXCTL	
-	4	6	-	10	10	17	PC2	I/O/A	-	PC2	ADC_IN12 TIM9_CH3N UART7_TX OPA3_CH1N ETH_MII_TXD2 ETH_RGMII_RXD0	
-	5	7	-	11	11	18	PC3	I/O/A	-	PC3	ADC_IN13 TIM10_CH3 UART7_RX OPA4_CH1N ETH_MII_TX_CLK ETH_RGMII_RXD1	
-	-	8	8	12	12	19	V_{SSA}	P	-	V_{SSA}		
-	-	-	-	-	-	20	V_{REF-}	P	-	V_{REF-}		
-	-	-	-	-	-	21	V_{REF+}	P	-	V_{REF+}		
-	-	9	9	13	13	22	V_{DDA}	P	-	V_{DDA}		
-	-	10	10	14	14	23	PA0-WKUP	I/O/A	-	PA0	WKUP USART2_CTS ADC_IN0 TIM2_CH1(14) TIM2_ETR(14) TIM5_CH1 TIM8_ETR OPA4_OUT0 ETH_MII_CRS ETH_RGMII_RXD2	TIM2_CH1_2(14) TIM2_ETR_2(14) TIM8_ETR_1
2	7	11	11	15	15	24	PA1(15)	I/O/A	-	PA1	USART2_RTS	TIM2_CH2_2

Pin No.							Pin name	Pin type(1)	I/O level	Main function (after reset)	Default alternate function	Remapping function(13)
TSSOP20	QFN28	LQFP48(V305CCT	LQFP48(V303CBT	LQFP64M	QFN68	LQFP100						
											ADC_IN1 TIM5_CH2 TIM2_CH2 OPA3_OUT0 ETH_MII_RX_CLK ETH_RMII_REF_CLK ETH_RGMII_RXD3	TIM9_BKIN_1
-	-	12	12	16	16	25	PA2	I/O/A	-	PA2	USART2_TX TIM5_CH3 ADC_IN2 TIM2_CH3 TIM9_CH1 TIM9_ETR OPA2_OUT0 ETH_MII_MDIO ETH_RMII_MDIO ETH_RGMII_GTXC	TIM2_CH3_1 TIM9_CH1_1 TIM9_ETR_1
-	-	-	-	-	17	-	V_{IO_4}	P	-	V_{IO_4}		
-	-	13	13	17	19	26	PA3	I/O/A	-	PA3	USART2_RX TIM5_CH4 ADC_IN3 TIM2_CH4 TIM9_CH2 OPA1_OUT0 ETH_MII_COL ETH_RGMII_TXEN	TIM2_CH4_1 TIM9_CH2_1
-	-	-	-	18	-	27	V_{SS_4}	P	-	V_{SS_4}		
-	-	-	-	19	-	28	V_{DD_4}	P	-	V_{DD_4}		
-	7	14	14	20	20	29	PA4	I/O/A	-	PA4	SPI1_NSS USART2_CK ADC_IN4 DAC1_OUT TIM9_CH3	SPI3_NSS_1 I2S3_WS_1 TIM9_CH3_1

Pin No.							Pin name	Pin type(1)	I/O level	Main function (after reset)	Default alternate function	Remapping function(13)
TSSOP20	QFN28	LQFP48(V305CCT	LQFP48(V303CBT	LQFP64M	QFN68	LQFP100						
											DVP_HSYNC	
2	8	15	15	21	21	30	PA5 (15)	I/O/A	-	PA5	SPI1_SCK ADC_IN5 DAC2_OUT OPA2_CH1N DVP_VSYNC	TIM10_CH1N_1 USART1_CTS_2 USART1_CK_3
-	9	16	16	22	22	31	PA6	I/O/A	-	PA6	SPI1_MISO TIM8_BKIN ADC_IN6 TIM3_CH1 OPA1_CH1N DVP_PCLK	TIM1_BKIN_1 USART1_TX_3 UART7_TX_1 TIM10_CH2N_1
-	10	17	17	23	23	32	PA7	I/O/A	-	PA7	SPI1_MOSI TIM8_CH1N ADC_IN7 TIM3_CH2 OPA2_CH1P ETH_MII_RX_DV ETH_RMII_CRS_DV ETH_RGMII_TXD0	TIM1_CH1N_1 USART1_RX_3 UART7_RX_1 TIM10_CH3N_1
-	-	18	-	24	24	33	PC4	I/O/A	-	PC4	ADC_IN14 TIM9_CH4 UART8_TX OPA4_CH1P ETH_MII_RXD0 ETH_RMII_RXD0 ETH_RGMII_TXD1	USART1_CTS_3
-	-	19	-	25	25	34	PC5	I/O/A	-	PC5	ADC_IN15 TIM9_BKIN UART8_RX OPA3_CH1P ETH_MII_RXD1 ETH_RMII_RXD1 ETH_RGMII_TXD2	USART1_RTS_3

Pin No.							Pin name	Pin type(1)	I/O level	Main function (after reset)	Default alternate function	Remapping function(13)
TSSOP20	QFN28	LQFP48(V305CCT	LQFP48(V303CBT	LQFP64M	QFN68	LQFP100						
-	-	20	18	26	26	35	PB0	I/O/A	-	PB0	ADC_IN8 TIM3_CH3 TIM8_CH2N OPA1_CH1P ETH_MII_RXD2 ETH_RGMII_TXD3	TIM1_CH2N_1 TIM3_CH3_2 TIM9_CH1N_1 UART4_TX_1
-	-	21	19	27	27	36	PB1	I/O/A	-	PB1	ADC_IN9 TIM3_CH4 TIM8_CH3N OPA4_CH0N ETH_MII_RXD3 ETH_RGMII_125IN	TIM1_CH3N_1 TIM3_CH4_2 TIM9_CH2N_1 UART4_RX_1
-	-	22	20	28	28	37	PB2(5)	I/O	FT	PB2 BOOT1(5)	OPA3_CH0N	TIM9_CH3N_1
-	-	-	-	-	-	38	PE7	I/O/A	FT	PE7	FSMC_D4 OPA3_OUT1	TIM1_ETR_3
-	-	-	-	-	-	39	PE8	I/O/A	FT	PE8	FSMC_D5 OPA4_OUT1	TIM1_CH1N_3 UART5_TX_2 UART5_TX_3
-	-	-	-	-	-	40	PE9	I/O	FT	PE9	FSMC_D6	TIM1_CH1_3 UART5_RX_2 UART5_RX_3
-	-	-	-	-	-	41	PE10	I/O	FT	PE10	FSMC_D7	TIM1_CH2N_3 UART6_TX_2 UART6_TX_3
-	-	-	-	-	-	42	PE11	I/O	FT	PE11	FSMC_D8	TIM1_CH2_3 UART6_RX_2 UART6_RX_3
-	-	-	-	-	-	43	PE12	I/O	FT	PE12	FSMC_D9	TIM1_CH3N_3 UART7_TX_2 UART7_TX_3
-	-	-	-	-	-	44	PE13	I/O	FT	PE13	FSMC_D10	TIM1_CH3_3 UART7_RX_2 UART7_RX_3
-	-	-	-	-	-	45	PE14	I/O/A	FT	PE14	FSMC_D11	TIM1_CH4_3

Pin No.							Pin name	Pin type(1)	I/O level	Main function (after reset)	Default alternate function	Remapping function(13)
TSSOP20	QFN28	LQFP48(V305CCT	LQFP48(V303CBT	LQFP64M	QFN68	LQFP100						
											OPA2_OUT1	UART8_TX_2 UART8_TX_3
-	-	-	-	-	-	46	PE15	I/O/A	FT	PE15	FSMC_D12 OPA1_OUT1	TIM1_BKIN_3 UART8_RX_2 UART8_RX_3
3	11	23	21	29	29	47	PB10	I/O/A	FT	PB10	I2C2_SCL USART3_TX OPA2_CH0N ETH_MII_RX_ER	TIM2_CH3_2 TIM2_CH3_3 TIM10_BKIN_1
4	12	24	22	30	30	48	PB11	I/O/A	FT	PB11	I2C2_SDA USART3_RX OPA1_CH0N ETH_MII_TX_EN ETH_RMII_TX_EN	TIM2_CH4_2 TIM2_CH4_3 TIM10_ETR_1
-	-	26	23	31	18	49	V_{SS_1}	P		V_{SS_1}		
-	-	-	-	32	31	50	V_{IO_1}	P		V_{IO_1}		
-	-	25	24	-	-	-	$V_{DD_IO_1}$	P		$V_{DD_IO_1}$		
-	-	-	-	-	32	-	V_{DD_1}	P		V_{DD_1}		
5	13	27	25	33	35	51	PB12	I/O/A	FT	PB12	SPI2_NSS I2S2_WS I2C2_SMBA USART3_CK TIM1_BKIN OPA4_CH0P CAN2_RX ETH_MII_TXD0 ETH_RMII_TXD0 ETH_RGMII_MDC	
6	14	28	26	34	36	52	PB13	I/O/A	FT	PB13	SPI2_SCK I2S2_CK USART3_CTS TIM1_CH1N OPA3_CH0P CAN2_TX ETH_MII_TXD1	USART3_CTS_1

Pin No.							Pin name	Pin type(1)	I/O level	Main function (after reset)	Default alternate function	Remapping function(13)
TSSOP20	QFN28	LQFP48(V305CCT	LQFP48(V303CBT	LQFP64M	QFN68	LQFP100						
											ETH_RMII_TXD1 ETH_RGMII_MDIO	
7	15	29	27	35	37	53	PB14	I/O/A	FT	PB14	SPI2_MISO TIM1_CH2N USART3_RTS OPA2_CH0P SDIO_D0(7)	USART3_RTS_1
8	16	30	28	36	38	54	PB15	I/O/A	FT	PB15	SPI2_MOSI I2S2_SD TIM1_CH3N OPA1_CH0P SDIO_D1(7)	USART1_TX_2
-	-	-	-	-	33	55	PD8	I/O	FT	PD8	FSMC_D13	USART3_TX_3 TIM9_CH1N_2 TIM9_CH1N_3 ETH_MII_RX_DV_1 ETH_RMII_CRS_DV_1
-	-	-	-	-	34	56	PD9	I/O	FT	PD9	FSMC_D14	USART3_RX_3 TIM9_CH1_2 TIM9_ETR_2 TIM9_CH1_3 TIM9_ETR_3 ETH_MII_RXD0_1 ETH_RMII_RXD0_1
-	-	-	-	-	-	57	PD10	I/O	FT	PD10	FSMC_D15	USART3_CK_2 USART3_CK_3 TIM9_CH2N_2 TIM9_CH2N_3 ETH_MII_RXD1_1 ETH_RMII_RXD1_1
-	-	-	-	-	-	58	PD11	I/O	FT	PD11	FSMC_A16	USART3_CTS_2

Pin No.							Pin name	Pin type(1)	I/O level	Main function (after reset)	Default alternate function	Remapping function(13)
TSSOP20	QFN28	LQFP48(V305CCT	LQFP48(V303CBT	LQFP64M	QFN68	LQFP100						
												USART3_CTS_3 TIM9_CH2_2 TIM9_CH2_3 ETH_MII_RXD2_1
-	-	-	-	-	-	59	PD12	I/O	FT	PD12	FSMC_A17	TIM4_CH1_1 TIM9_CH3N_2 TIM9_CH3N_3 USART3_RTS_3 ETH_MII_RXD3 USART3_RTS_2
-	-	-	-	-	-	60	PD13	I/O	FT	PD13	FSMC_A18	TIM4_CH2_1 TIM9_CH3_2 TIM9_CH3_3
-	-	-	-	-	-	61	PD14	I/O	FT	PD14	FSMC_D0	TIM4_CH3_1 TIM9_BKIN_2 TIM9_BKIN_3
-	-	-	-	-	-	62	PD15	I/O	FT	PD15	FSMC_D1	TIM4_CH4_1 TIM9_CH4_2 TIM9_CH4_3
9	-	31	-	37	39	63	PC6	I/O	FT	PC6	I2S2_MCK TIM8_CH1 SDIO_D6 ETH_RXP	TIM3_CH1_3
10	-	-	-	38	40	64	PC7	I/O	FT	PC7	I2S3_MCK(11) (12) TIM8_CH2 SDIO_D7 ETH_RXN	TIM3_CH2_3
11	17	-	-	39	41	65	PC8	I/O	FT	PC8	TIM8_CH3 SDIO_D0(7) ETH_TXP DVP_D2	TIM3_CH3_3
12	18	-	-	40	42	66	PC9 (6)	I/O	FT	PC9	TIM8_CH4 SDIO_D1(7) ETH_TXN DVP_D3	TIM3_CH4_3
		32	29	41	43	67	PA8(6)	I/O	FT	PA8	USART1_CK	USART1_CK_1

Pin No.							Pin name	Pin type(1)	I/O level	Main function (after reset)	Default alternate function	Remapping function(13)
TSSOP20	QFN28	LQFP48(V305CCT	LQFP48(V303CBT	LQFP64M	QFN68	LQFP100						
											TIM1_CH1 MCO I2S3_MCK(11) (12)	USART1_RX_2 TIM1_CH1_1
13	-	33	30	42	44	68	PA9(16)	I/O	FT	PA9	USART1_TX TIM1_CH2 OTG_FS_VBUS DVP_D0 I2S3_SD(10) (12)	USART1_RTS_2 TIM1_CH2_1
-	-	34	31	43	45	69	PA10	I/O	FT	PA10	USART1_RX TIM1_CH3 OTG_FS_ID DVP_D1	USART1_CK_2 TIM1_CH3_1
-	-	35	32	44	46	70	PA11	I/O/A	FT	PA11	USART1_CTS CAN1_RX TIM1_CH4 OTG_FS_DM	USART1_CTS_1 TIM1_CH4_1
-	-	36	33	45	47	71	PA12	I/O/A	FT	PA12	USART1_RTS CAN1_TX TIM1_ETR TIM10_CH1N OTG_FS_DP	USART1_RTS_1 TIM1_ETR_1
13	19	37	34	46	48	72	PA13(16)	I/O	FT	SWDIO	TIM10_CH2N	PA13 TIM8_CH1N_1 USART3_TX_2
-	-	-	-	-	-	73	Unused					
-	-	-	35	47	49	74	V_{SS_2}	P	-	V_{SS_2}		
-	-	-	36	48	50	75	V_{DD_2}	P	-	V_{DD_2}		
-	-	-	-	-	51	-	V_{IO_2}	P	-	V_{IO_2}		
15	22	38	37	49	52	76	PA14	I/O	FT	SWCLK	TIM10_CH3N	TIM8_CH2N_1 UART8_TX_1 PA14 USART3_RX_2
-	-	39	38	50	53	77	PA15	I/O	FT	PA15	SPI3_NSS(12) SPI3_MOSI(12) I2S3_WS(12)	TIM2_CH1_1(14) TIM2_ETR_1(14) TIM2_CH1_3(14) TIM2_ETR_3(14) SPI1_NSS_1

Pin No.							Pin name	Pin type[1]	I/O level	Main function (after reset)	Default alternate function	Remapping function[13]
TSSOP20	QFN28	LQFP48(V305CCT	LQFP48(V303CBT	LQFP64M	QFN68	LQFP100						
												TIM8_CH3N_1 UART8_RX_1
-	23	-	-	51	54	78	PC10	I/O	FT	PC10	UART4_TX SDIO_D2 TIM10_ETR DVP_D8	USART3_TX_1 SPI3_SCK_1 I2S3_CK_1
-	24	-	-	52	55	79	PC11	I/O	FT	PC11	UART4_RX SDIO_D3 TIM10_CH4 DVP_D4	USART3_RX_1 SPI3_MISO_1
-	25	-	-	53	56	80	PC12	I/O	FT	PC12	UART5_TX SDIO_CK TIM10_BKIN DVP_D9	USART3_CK_1 SPI3_MOSI_1 I2S3_SD_1
-	-	-	-	-	-	81	PD0	I/O/A	FT	PD0	FSMC_D2	CAN1_RX_3 TIM10_ETR_2 TIM10_ETR_3
-	-	-	-	-	-	82	PD1	I/O/A	FT	PD1	FSMC_D3	CAN1_TX_3 TIM10_CH1_2 TIM10_CH1_3
-	26	-	-	54	57	83	PD2	I/O	FT	PD2	TIM3_ETR UART5_RX SDIO_CMD DVP_D11 FSMC_NADV[9]	TIM3_ETR_2 TIM3_ETR_3
-	-	-	-	-	-	84	PD3	I/O	FT	PD3	FSMC_CLK	USART2_CTS_1 TIM10_CH2_2 TIM10_CH2_3
-	-	-	-	-	-	85	PD4	I/O	FT	PD4	FSMC_NOE	USART2_RTS_1
-	-	-	-	-	-	86	PD5	I/O	FT	PD5	FSMC_NWE	USART2_TX_1 TIM10_CH3_2 TIM10_CH3_3
-	-	-	-	-	-	87	PD6	I/O	FT	PD6	FSMC_NWAIT DVP_D10	USART2_RX_1
-	-	-	-	-	-	88	PD7	I/O	FT	PD7	FSMC_NE1 FSMC_NCE2	USART2_CK_1 TIM10_CH4_2 TIM10_CH4_3

Pin No.							Pin name	Pin type(1)	I/O level	Main function (after reset)	Default alternate function	Remapping function(13)
TSSOP20	QFN28	LQFP48(V305CCT	LQFP48(V303CBT	LQFP64M	QFN68	LQFP100						
-	-	40	39	55	58	89	PB3	I/O	FT	PB3	SPI3_SCK I2S3_CK(12) DVP_D5(8)	TIM2_CH2_1 TIM2_CH2_3 SPI1_SCK_1 TIM10_CH1_1
-	-	41	40	56	59	90	PB4	I/O	FT	PB4	SPI3_MISO	TIM3_CH1_2 SPI1_MISO_1 UART5_TX_1 TIM10_CH2_1
-	-	42	41	57	60	91	PB5	I/O	FT	PB5	I2C1_SMBA SPI3_MOSI(12) I2S3_SD(10) (12) ETH_MII_PPS_OUT ETH_RMII_PPS_OUT	TIM3_CH2_2 SPI1_MOSI_1 CAN2_RX_1 TIM10_CH3_1 UART5_RX_1
16	27	43	42	58	61	92	PB6	I/O	FT	PB6	I2C1_SCL TIM4_CH1 USBFS_DM DVP_D5(8) USBHS_DM	USART1_TX_1 CAN2_TX_1 TIM8_CH1_1
17	28	44	43	59	62	93	PB7	I/O	FT	PB7	I2C1_SDA FSMC_NADV TIM4_CH2 USBFS_DP USBHS_DP	USART1_RX_1 TIM8_CH2_1
-	-	-	44	60	63	94	BOOT0(5)	I	-	BOOT0(5)		
-	-	45	45	61	64	95	PB8	I/O/A	FT	PB8	TIM4_CH3 SDIO_D4 TIM10_CH1 DVP_D6 ETH_MII_TXD3	I2C1_SCL_1 CAN1_RX_2 UART6_TX_1 TIM8_CH3_1
-	-	46	46	62	65	96	PB9	I/O/A	FT	PB9	TIM4_CH4 SDIO_D5 TIM10_CH2 DVP_D7	I2C1_SDA_1 CAN1_TX_2 UART6_RX_1 TIM8_BKIN_1
-	-	-	-	-	66	97	PE0	I/O	FT	PE0	TIM4_ETR FSMC_NBL0	TIM4_ETR_1 UART4_TX_2

Pin No.							Pin name	Pin type(1)	I/O level	Main function (after reset)	Default alternate function	Remapping function(13)
TSSOP20	QFN28	LQFP48(V305CCT	LQFP48(V303CBT	LQFP64M	QFN68	LQFP100						
												UART4_TX_3
-	-	-	-	-	-	98	PE1	I/O	FT	PE1	FSMC_NBL1	UART4_RX_2 UART4_RX_3
-	-	47	47	63	-	99	V_{SS_3}	P	-	V_{SS_3}		
-	-	-	-	64	67	100	V_{IO_3}	P	-	V_{IO_3}		
-	-	-	-	-	68	-	V_{DD_3}	P	-	V_{DD_3}		
-	-	48	48	-		-	$V_{DD_IO_3}$	P	-	$V_{DD_IO_3}$		
14	21	-	-	-	-	-	V_{DD}	P	-	V_{DD}		
	6	-	-	-	-	-	V_{IO}	P	-	V_{IO}		

Note 1: Abbreviations in the table

I = TTL/CMOS Schmitt input;

O = CMOS tri-state output;

A = analog signal input or output;

P = power;

FT = 5V tolerance;

ANT = RF signal input and output (antenna).

Note 2: Both V_{DD} and V_{BAT} can be connected with an internal analog switch to supply power to the backup area and the pins PC13, PC14 and PC15. This analog switch can only pass a limited current (3mA). When powered by V_{DD}, PC14 and PC15 can be used for GPIO or LSE pins, and PC13 can be used as a general-purpose I/O port, TAMPER pin, RTC calibration clock, RTC alarm clock or second output; PC13, PC14 and PC15 can only work in 2MHz mode when they are used as GPIO output pins, and the maximum driving load is 30pF, and they cannot be used as current sources (such as driving LEDs). When the power is supplied by V_{BAT}, PC14 and PC15 can only be used for LSE pin, and PC13 can be used as TAMPER pin, RTC alarm clock or second output.

Note 3: These pins are in the main function state when the backup area is powered on for the first time. Even after reset, the state of these pins is controlled by the backup area registers (these registers will not be reset by the main reset system). For specific information on how to control these I/O ports, please refer to the relevant chapters on the battery backup area and BKP register in the CH32FV2x_V3xRM datasheet.

Note 4: Pin 5 and pin 6 of those in LQFP64M package are configured as OSC_IN and OSC_OUT function pins by default after chip reset. Software can reconfigure these 2 pins as PD0 and PD1. But for those in LQFP100 package, since PD0 and PD1 are inherent functional pins, there is no need to remap settings by software. For more detailed information, please refer to the chapters on Alternate Function I/O and Debug Setting in the CH32FV2x_V3xRM datasheet.

Note 5: For devices without the BOOT0 pinout, they are pulled down to GND internally. For devices with the BOOT0 pinout but no BOOT1/PB2 pinout, BOOT1/PB2 is pulled down to GND internally. In this case, it is recommended that the BOOT1/PB2 pinout is set to input pull-down mode if a device goes into the low-power mode and configures I/O port state, to avoid generating extra current.

Note 6: For CH32V305FBP6 and CH32V305GBU6 chips, the PA8 and PC9 pins are shorted inside the chip, it

is prohibited to configure both IOs as output functions, pay attention to the pin state if there are power consumption requirements.

Note 7: SDIO_D0 and SDIO_D1 are mapped to PC8 and PC9 by default. Only for products with the fifth from the bottom of the batch number greater than 1 or the sixth from the bottom of the lot number not equal to 0 (except for the chip CH32V305GBU6), when the bit[14]ETHMACEN=1 and bit[10]SDIOEN=1 in the register RCC_AHBPCENR, the default mapping of SDIO_D0 and SDIO_D1 is automatically changed to PB14 and PB15.

Note 8: DVP_D5 is mapped to PB6 by default. Only for products with the fifth from the bottom of the lot number greater than 1 or the sixth from the bottom of the batch number not equal to 0, when the bit[13]DVPEN=1 and bit[11]USBHSEN=1 in the register RCC_AHBPCENR and the bit[2]RB_UC_RST_SIE=0 in R8_USB_CTRL, the default mapping of DVP_D5 is automatically changed to PB3.

Note 9: FSMC_NADV is mapped to PB7 by default. Only for products with the fifth from the bottom of the lot number greater than 1 or the sixth from the bottom of the lot number not equal to 0, when the bit[8]FSMCEN=1 and bit[11]USBHSEN=1 in the register RCC_AHBPCENR and bit[2]RB_UC_RST_SIE=0 in R8_USB_CTRL, the default mapping of FSMC_NADV will be automatically changed to.

Note 10: I2S3_SD is mapped to PB5 by default. Only for products with the fifth from the bottom of the lot number greater than 2 or the sixth last digit of the lot number not equal to 0, if 10M Ethernet and I2S3 functions are used at the same time, the default mapping of I2S3_SD will be automatically changed to PA9.

Note 11: I2S3_MCK is mapped to PC7 by default. Only for products with the fifth from the bottom of the lot number greater than 2 or the sixth last digit of the lot number not equal to 0, if 10M Ethernet and I2S3 functions are used at the same time, the default mapping of I2S3_MCK will be automatically changed to PA8.

Note 12: SPI3_MOSI is mapped to PB5 by default. Only for products with the fifth from the bottom of the lot number equal to 2 or the sixth last digit of the lot number equal to 0, when using Ethernet, the default pin function of I2S3 is not available, and the chip selection signal of the default pin of SPI3 is not available. At this time, the default mapping of SPI3_MOSI is automatically changed to PA15.

Note 13: The value after the underscore of the remap function indicates the configuration value of the corresponding bit in the AFIO register. For example, UART4_RX_3 indicates that the corresponding bit in the AFIO register is configured as 11b.

Note 14: TIM2_CH1 and TIM2_ETR share a common pin, but cannot be used at the same time.

Note 15 and Note 16: For CH32V305FBP6 chip, PA5 and PA1 pins are short-circuited inside the chip, prohibiting both IOs to be configured as output function; PA9 and PA13 pins are short-circuited inside the chip, prohibiting both IOs to be configured as output function; pay attention to the pin status if there is power consumption requirement.

Table 3-2 CH32V317 pin definitions

Pin No.		Pin name	Pin type(1)	I/O level	Main function (after reset)	Default alternate function	Remapping function(13)
QFN68	LQFP10						
0	-	VSS	P	-	VSS		
-	1	PE2	I/O	FT	PE2		TIM10_BKIN_2 TIM10_BKIN_3
-	2	PE3	I/O	FT	PE3		TIM10_CH1N_2 TIM10_CH1N_3
-	3	PE4	I/O	FT	PE4		TIM10_CH2N_2

Pin No.		Pin name	Pin type(1)	I/O level	Main function (after reset)	Default alternate function	Remapping function(13)
QFN68	LQFP10						
							TIM10_CH2N_3
-	4	PE5	I/O	FT	PE5		TIM10_CH3N_2 TIM10_CH3N_3
-	5	PE6	I/O	FT	PE6		
1	6	V_{BAT}	P	-	V_{BAT}		
2	7	PC13-TAMPER-RTC(2)	I/O	-	PC13(3)	TAMPER-RTC	TIM8_CH4_1
3	8	PC14-OSC32_IN(2)	I/O/A	-	PC14(3)	OSC32_IN	TIM9_CH4_1
4	9	PC15-OSC32_OUT(2)	I/O/A	-	PC15(3)	OSC32_OUT	TIM10_CH4_1
-	10	V_{SS_5}	P	-	V_{SS_5}		
-	11	V_{DD_5}	P	-	V_{DD_5}		
5	12	OSC_IN	I/A	-	OSC_IN		PD0(4)
6	13	OSC_OUT	O/A	-	OSC_OUT		PD1(4)
7	14	NRST	I	-	NRST		
8	15	PC0	I/O/A	-	PC0	ADC_IN10 TIM9_CH1N UART6_TX	
9	16	PC1	I/O/A	-	PC1	ADC_IN11 TIM9_CH2N UART6_RX	
10	17	PC2	I/O/A	-	PC2	ADC_IN12 TIM9_CH3N UART7_TX OPA3_CH1N	
11	18	PC3	I/O/A	-	PC3	ADC_IN13 TIM10_CH3 UART7_RX OPA4_CH1N	
12	19	V_{SSA}	P	-	V_{SSA}		
-	20	V_{REF-}	P	-	V_{REF-}		
-	21	V_{REF+}	P	-	V_{REF+}		
13	22	V_{DDA}	P	-	V_{DDA}		
14	23	PA0-WKUP	I/O/A	-	PA0	WKUP USART2_CTS ADC_IN0	TIM2_CH1_2(11) TIM2_ETR_2(11) TIM8_ETR_1

Pin No.		Pin name	Pin type[1]	I/O level	Main function (after reset)	Default alternate function	Remapping function[13]
QFN68	LQFP10						
						TIM2_CH1[11] TIM2_ETR[11] TIM5_CH1 TIM8_ETR OPA4_OUT0	
15	24	PA1	I/O/A	-	PA1	USART2_RTS ADC_IN1 TIM5_CH2 TIM2_CH2 OPA3_OUT0	TIM2_CH2_2 TIM9_BKIN_1
16	25	PA2	I/O/A	-	PA2	USART2_TX TIM5_CH3 ADC_IN2 TIM2_CH3 TIM9_CH1 TIM9_ETR OPA2_OUT0	TIM2_CH3_1 TIM9_CH1_1 TIM9_ETR_1
17	26	PA3	I/O/A	-	PA3	USART2_RX TIM5_CH4 ADC_IN3 TIM2_CH4 TIM9_CH2 OPA1_OUT0	TIM2_CH4_1 TIM9_CH2_1
-	27	V_{SS_4}	P	-	V_{SS_4}		
18	28	V_{IO_4}	P	-	V_{IO_4}		
19	29	PA4	I/O/A	-	PA4	SPI1_NSS USART2_CK ADC_IN4 DAC1_OUT TIM9_CH3 DVP_HSYNC	SPI3_NSS_1 I2S3_WS_1 TIM9_CH3_1
20	30	PA5	I/O/A	-	PA5	SPI1_SCK ADC_IN5 DAC2_OUT OPA2_CH1N DVP_VSYNC	TIM10_CH1N_1 USART1_CTS_2 USART1_CK_3
21	31	PA6	I/O/A	-	PA6	SPI1_MISO TIM8_BKIN ADC_IN6 TIM3_CH1	TIM1_BKIN_1 USART1_TX_3 UART7_TX_1 TIM10_CH2N_1

Pin No.		Pin name	Pin type[1]	I/O level	Main function (after reset)	Default alternate function	Remapping function[13]
QFN68	LQFP10						
						OPA1_CH1N DVP_PCLK	
22	32	PA7	I/O/A	-	PA7	SPI1_MOSI TIM8_CH1N ADC_IN7 TIM3_CH2 OPA2_CH1P	TIM1_CH1N_1 USART1_RX_3 UART7_RX_1 TIM10_CH3N_1
23	33	PC4	I/O/A	-	PC4	ADC_IN14 TIM9_CH4 UART8_TX OPA4_CH1P	USART1_CTS_3
24	34	PC5	I/O/A	-	PC5	ADC_IN15 TIM9_BKIN UART8_RX OPA3_CH1P	USART1_RTS_3
25	35	PB0	I/O/A	-	PB0	ADC_IN8 TIM3_CH3 TIM8_CH2N OPA1_CH1P	TIM1_CH2N_1 TIM3_CH3_2 TIM9_CH1N_1 UART4_TX_1
26	36	PB1	I/O/A	-	PB1	ADC_IN9 TIM3_CH4 TIM8_CH3N OPA4_CH0N	TIM1_CH3N_1 TIM3_CH4_2 TIM9_CH2N_1 UART4_RX_1
27	37	PB2[5]	I/O	FT	PB2 BOOT1[5]	OPA3_CH0N	TIM9_CH3N_1
28	38	LED0	I/O	-	LED0		
29	39	LED1	I/O	-	LED1		
30	40	V_{DDK}	P	-	V_{DDK}		
-	41	V_{SS_6}	P	-	V_{SS_6}		
31	42	MDITP	I/O	-	MDITP		
32	43	MDITN	I/O	-	MDITN		
33	44	MDIRP	I/O	-	MDIRP		
34	45	MDIRN	I/O	-	MDIRN		
35	46	V_{DD_ETH}	P	-	V_{DD_ETH}		
-	47	V_{SS_1}	P	-	V_{SS_1}		
36	48	V_{IO_1}	P	-	V_{IO_1}		
42	49	PB10[6]	I/O/A	FT	PB10	I2C2_SCL USART3_TX OPA2_CH0N	TIM2_CH3_2 TIM2_CH3_3 TIM10_BKIN_1
41	50	PB11[7]	I/O/A	FT	PB11	I2C2_SDA	TIM2_CH4_2

Pin No.		Pin name	Pin type[1]	I/O level	Main function (after reset)	Default alternate function	Remapping function[13]
QFN68	LQFP10						
						USART3_RX OPA1_CH0N	TIM2_CH4_3 TIM10_ETR_1
-	51	V_{DD_1}	P		V_{DD_1}		
37	52	PB12	I/O/A	FT	PB12	SPI2_NSS I2S2_WS I2C2_SMBA USART3_CK TIM1_BKIN OPA4_CH0P CAN2_RX	
38	53	PB13	I/O/A	FT	PB13	SPI2_SCK I2S2_CK USART3_CTS TIM1_CH1N OPA3_CH0P CAN2_TX	USART3_CTS_1
39	54	PB14	I/O/A	FT	PB14	SPI2_MISO TIM1_CH2N USART3_RTS OPA2_CH0P SDIO_D0[8]	USART3_RTS_1
40	55	PB15	I/O/A	FT	PB15	SPI2_MOSI I2S2_SD TIM1_CH3N OPA1_CH0P SDIO_D1[8]	USART1_TX_2
-	56	PD9	I/O	FT	PD9		USART3_RX_3 TIM9_CH1_2 TIM9_ETR_2 TIM9_CH1_3 TIM9_ETR_3
-	57	PD10	I/O	FT	PD10		USART3_CK_2 USART3_CK_3 TIM9_CH2N_2 TIM9_CH2N_3
-	58	PD11	I/O	FT	PD11		USART3_CTS_2 USART3_CTS_3 TIM9_CH2_2 TIM9_CH2_3
-	59	PD12	I/O	FT	PD12		TIM4_CH1_1

Pin No.		Pin name	Pin type(1)	I/O level	Main function (after reset)	Default alternate function	Remapping function(13)
QFN68	LQFP10						
							TIM9_CH3N_2 TIM9_CH3N_3 USART3_RTS_3 USART3_RTS_2
-	60	PD13	I/O	FT	PD13		TIM4_CH2_1 TIM9_CH3_2 TIM9_CH3_3
41	61	PD14 (7)	I/O	FT	PD14		TIM4_CH3_1 TIM9_BKIN_2 TIM9_BKIN_3
42	62	PD15 (6)	I/O	FT	PD15		TIM4_CH4_1 TIM9_CH4_2 TIM9_CH4_3
-	63	PC6	I/O	FT	PC6	I2S2_MCK TIM8_CH1 SDIO_D6	TIM3_CH1_3
-	64	PC7	I/O	FT	PC7	I2S3_MCK TIM8_CH2 SDIO_D7	TIM3_CH2_3
-	65	PC8	I/O	FT	PC8	TIM8_CH3 SDIO_D0 (8) DVP_D2	TIM3_CH3_3
-	66	PC9	I/O	FT	PC9	TIM8_CH4 SDIO_D1 (8) DVP_D3	TIM3_CH4_3
43	67	PA8	I/O	FT	PA8	USART1_CK TIM1_CH1 MCO	USART1_CK_1 USART1_RX_2 TIM1_CH1_1
44	68	PA9	I/O	FT	PA9	USART1_TX TIM1_CH2 OTG_FS_VBUS DVP_D0	USART1_RTS_2 TIM1_CH2_1
45	69	PA10	I/O	FT	PA10	USART1_RX TIM1_CH3 OTG_FS_ID DVP_D1	USART1_CK_2 TIM1_CH3_1
46	70	PA11	I/O/A	FT	PA11	USART1_CTS CAN1_RX TIM1_CH4 OTG_FS_DM	USART1_CTS_1 TIM1_CH4_1

Pin No.		Pin name	Pin type[1]	I/O level	Main function (after reset)	Default alternate function	Remapping function[13]
QFN68	LQFP10						
47	71	PA12	I/O/A	FT	PA12	USART1_RTS CAN1_TX TIM1_ETR TIM10_CH1N OTG_FS_DP	USART1_RTS_1 TIM1_ETR_1
48	72	PA13	I/O	FT	SWDIO	TIM10_CH2N	PA13 TIM8_CH1N_1 USART3_TX_2
-	73	NC.					
49	74	V_{SS_2}	P	-	V_{SS_2}		
50	75	V_{DD_2}	P	-	V_{DD_2}		
51	-	V_{IO_2}	P	-	V_{IO_2}		
52	76	PA14	I/O	FT	SWCLK	TIM10_CH3N	TIM8_CH2N_1 UART8_TX_1 PA14 USART3_RX_2
53	77	PA15	I/O	FT	PA15	SPI3_NSS I2S3_WS	TIM2_CH1_1[11] TIM2_ETR_1[11] TIM2_CH1_3[11] TIM2_ETR_3[11] SPI1_NSS_1 TIM8_CH3N_1 UART8_RX_1
54	78	PC10	I/O	FT	PC10	UART4_TX SDIO_D2 TIM10_ETR DVP_D8	USART3_TX_1 SPI3_SCK_1 I2S3_CK_1
55	79	PC11	I/O	FT	PC11	UART4_RX SDIO_D3 TIM10_CH4 DVP_D4	USART3_RX_1 SPI3_MISO_1
56	80	PC12	I/O	FT	PC12	UART5_TX SDIO_CK TIM10_BKIN DVP_D9	USART3_CK_1 SPI3_MOSI_1 I2S3_SD_1
-	81	PD0	I/O/A	FT	PD0		CAN1_RX_3 TIM10_ETR_2 TIM10_ETR_3
-	82	PD1	I/O/A	FT	PD1		CAN1_TX_3 TIM10_CH1_2

Pin No.		Pin name	Pin type[1]	I/O level	Main function (after reset)	Default alternate function	Remapping function[13]
QFN68	LQFP10						
							TIM10_CH1_3
57	83	PD2	I/O	FT	PD2	TIM3_ETR UART5_RX SDIO_CMD DVP_D11	TIM3_ETR_2 TIM3_ETR_3
-	84	PD3	I/O	FT	PD3		USART2_CTS_1 TIM10_CH2_2 TIM10_CH2_3
-	85	PD4	I/O	FT	PD4		USART2_RTS_1
-	86	PD5	I/O	FT	PD5		USART2_TX_1 TIM10_CH3_2 TIM10_CH3_3
-	87	PD6	I/O	FT	PD6	DVP_D10	USART2_RX_1
-	88	PD7	I/O	FT	PD7		USART2_CK_1 TIM10_CH4_2 TIM10_CH4_3
58	89	PB3	I/O	FT	PB3	SPI3_SCK I2S3_CK DVP_D5[9]	TIM2_CH2_1 TIM2_CH2_3 SPI1_SCK_1 TIM10_CH1_1
59	90	PB4	I/O	FT	PB4	SPI3_MISO	TIM3_CH1_2 SPI1_MISO_1 UART5_TX_1 TIM10_CH2_1
60	91	PB5	I/O	FT	PB5	I2C1_SMBA SPI3_MOSI I2S3_SD	TIM3_CH2_2 SPI1_MOSI_1 CAN2_RX_1 TIM10_CH3_1 UART5_RX_1
61	92	PB6	I/O	FT	PB6	I2C1_SCL TIM4_CH1 USBFS_DM DVP_D5[9] USBHS_DM	USART1_TX_1 CAN2_TX_1 TIM8_CH1_1
62	93	PB7	I/O	FT	PB7	I2C1_SDA TIM4_CH2 USBFS_DP USBHS_DP	USART1_RX_1 TIM8_CH2_1
63	94	BOOT0[5]	I	-	BOOT0[5]		

Pin No.		Pin name	Pin type(1)	I/O level	Main function (after reset)	Default alternate function	Remapping function(13)
QFN68	LQFP10						
64	95	PB8	I/O/A	FT	PB8	TIM4_CH3 SDIO_D4 TIM10_CH1 DVP_D6	I2C1_SCL_1 CAN1_RX_2 UART6_TX_1 TIM8_CH3_1
65	96	PB9	I/O/A	FT	PB9	TIM4_CH4 SDIO_D5 TIM10_CH2 DVP_D7	I2C1_SDA_1 CAN1_TX_2 UART6_RX_1 TIM8_BKIN_1
66	97	PE0	I/O	FT	PE0	TIM4_ETR	TIM4_ETR_1 UART4_TX_2 UART4_TX_3
-	98	PE1	I/O	FT	PE1		UART4_RX_2 UART4_RX_3
-	99	V_{SS_3}	P	-	V_{SS_3}		
67	100	V_{IO_3}	P	-	V_{IO_3}		
68	-	V_{DD_3}	P	-	V_{DD_3}		

Note 1: Abbreviations in the table

I = TTL/CMOS Schmitt input;

O = CMOS tri-state output;

A = analog signal input or output;

P = power;

FT = 5V tolerance;

Note 2: Both V_{DD} and V_{BAT} can be connected with an internal analog switch to supply power to the backup area and the pins PC13, PC14 and PC15. This analog switch can only pass a limited current (3mA). When powered by V_{DD}, PC14 and PC15 can be used for GPIO or LSE pins, and PC13 can be used as a general-purpose I/O port, TAMPER pin, RTC calibration clock, RTC alarm clock or second output; PC13, PC14 and PC15 can only work in 2MHz mode when they are used as GPIO output pins, and the maximum driving load is 30pF, and they cannot be used as current sources (such as driving LEDs). When the power is supplied by V_{BAT}, PC14 and PC15 can only be used for LSE pin, and PC13 can be used as TAMPER pin, RTC alarm clock or second output.

Note 3: These pins are in the main function state when the backup area is powered on for the first time. Even after reset, the state of these pins is controlled by the backup area registers (these registers will not be reset by the main reset system). For specific information on how to control these I/O ports, please refer to the relevant chapters on the battery backup area and BKP register in the CH32FV2x_V3xRM datasheet.

Note 4: For CH32V317WCU6 chip, pin 5 and pin 6 are configured as OSC_IN and OSC_OUT function pins by default after the chip is reset. Software can reset these two pins to PD0 and PD1 functions. However, for CH32V317VCT6 chip, because PD0 and PD1 are inherent function pins, there is no need for remapping settings by software. For more details, please refer to the reuse function I/O chapter and debugging setting chapter in the CH32FV2x_V3xRM.

Note 5: The chip with the BOOT0 pin not led out will be pulled down to GND internally. At this time, if the IO port is configured in low power mode, it is suggested that the input pull-down mode be used for the BOOT1/PB2

pin to prevent additional current.

Note 6, note 7: For CH32V317WCU6 chip, the pins PB10 and PD15 are short sealed inside the chip, and it is forbidden to configure both IO as output function, so pay attention to the pin state with power consumption requirements; PB11 and PD14 pins are short-sealed inside the chip, so it is forbidden to configure both IO as output function. Please pay attention to the pin status if there is power consumption requirement.

Note 8: SDIO_D0 and SDIO_D1 are mapped to PC8 and PC9 by default. When bit[14]ETHMACEN=1 and bit[10]SDIOEN=1 in register RCC_AHBPCENR, the default mapping of SDIO_D0 and SDIO_D1 is automatically changed to PB14 and PB15.

Note 9: DVP_D5 is mapped to PB6 by default. When bit[13]DVPEN=1 and bit[11]USBHSEN=1 in register RCC_AHBPCENR and bit[2]RB_UC_RST_SIE=0 in R8_USB_CTRL, the default mapping of DVP_D5 is automatically changed to PB3.

Note 10: The value underlined by the remapping function indicates the configuration value of the corresponding bit in the AFIO register. For example, UART4_RX_3 indicates that the corresponding bit of AFIO register is configured as 11b.

Note 11: TIM2_CH1 and TIM2_ETR share a pin, but they cannot be used at the same time.

Table 3-3 CH32V317 proprietary pin description

<table>
<tr><th>Pin name</th><th>Pin description</th></tr>
<tr><td>V_{DD_ETH}</td><td>To supply power to the 10/100M Ethernet PHY, it is suggested that the capacitance between 1UF and 4.7UF should be placed close to the chip, which supports 10uF but needs to be connected in parallel with 0.1uF.</td></tr>
<tr><td>V_{DDK}</td><td>The external 1uF capacitor to ground is placed close to the chip.</td></tr>
<tr><td>MDITP
MDITN</td><td>Differential output in 10BASE-T/100BASE-TX MDI mode;
Differential input in 10BASE-T/100BASE-TX MDIX mode.</td></tr>
<tr><td>MDIRP
MDIRN</td><td>Differential input in 10BASE-T/100BASE-TX MDI mode;
Differential output in 10BASE-T/100BASE-TX MDIX mode.</td></tr>
<tr><td>LED0</td><td>Traditional LED function selection, the default LED_SEL is 11:
<table>
<tr><th>LED_SEL</th><th>00</th><th>01</th><th>10</th><th>11</th></tr>
<tr><td>LED0</td><td>ACT_{ALL}</td><td>$LINK_{ALL}$ /ACT_{ALL}</td><td>$LINK_{10}$ /ACT_{ALL}</td><td>$LINK_{10}$ /ACT_{10}</td></tr>
</table></td></tr>
<tr><td>LED1</td><td>Traditional LED function selection, the default LED_SEL is 11:
<table>
<tr><th>LED_SEL</th><th>00</th><th>01</th><th>10</th><th>11</th></tr>
<tr><td>LED1</td><td>$LINK_{100}$</td><td>$LINK_{100}$</td><td>$LINK_{100}$</td><td>$LINK_{100}$ /ACT_{100}</td></tr>
</table></td></tr>
</table>

3.3 Pin Alternate Functions

Note: The pin function in the table below refer to all functions and does not involve specific model(s). There are differences in peripheral resources between different models. Please confirm whether this function is available according to the particular model's resource table before viewing this table.

Table 3-4 Pin alternate and remapping functions

Alternate / Pin	ADC DAC	TIM1 8/9/10	TIM2 3/4/5	UART USART	USB	SYS	I2C	SPI I2S	ETH	FSMC SDIO	DVP	OPA	CAN
PA0	ADC_IN0	TIM8_ETR TIM8_ETR_1	TIM2_CH1 TIM2_ETR TIM2_CH1_2 TIM2_ETR_2 TIM5_CH1	USART2_CTS		WKUP			ETH_MII_CRS ETH_RGMII_RXD2			0PA4_OUT0	
PA1	ADC_1N1	TIM9_BKIN_1	TIM2_CH2 TIM2_CH2_2 TIM5_CH2	USART2_RTS					ETH_MII_RX_CLK ETH_RMII_REF_CLK ETH_RGMII_RXD3			OPA3_OUT0	
PA2	ADC_IN2	TIM9_CH1 TIM9_CH1_1 TIM9_ETR TIM9_ETR_1	TIM2_CH3 TIM2_CH3_1 TIM5_CH3	USART2_TX					ETH_MII_MDIO ETH_RMII_MDIO ETH_RGMII_GTXC			OPA2_OUT0	
PA3	ADC_IN3	TIM9_CH2 TIM9_CH2_1	TIM2_CH4 TIM2_CH4_1 TIM5_CH4	USART2_RX					ETH_MII_COL ETH_RGMII_TXEN			OPA1_OUT0	
PA4	ADC_IN4 DAC1_OUT	TIM9_CH3 TIM9_CH3_1		USART2_CK				SPI1_NSS SPI3_NSS_1 I2S3_WS_1			DVP_HSYNC		
PA5	ADC_IN5 DAC2_OUT	TIM10_CH1N_1		USART1_CTS_2 USART1_CK_3				SPI1_SCK			DVP_VSYNC	OPA2_CH1N	
PA6	ADC_IN6	TIM1_BKIN_1 TIM8_BKIN TIM10_CH2N_1	TIM3_CH1	USART1_TX_3 UART7_TX_1				SPI1_MISO			DVP_PCLK	OPA1_CH1N	
PA7	ADC_IN7	TIM1_CH1N_1 TIM8_CH1N TIM10_CH3N_1	TIM3_CH2	USART1_RX_3 UART7_RX_1				SPI1_MOSI	ETH_MII_RX_DV ETH_RMII_CRS_DV ETH_RGMII_TXD0			OPA2_CH1P	
PA8		TIM1_CH1 TIM1_CH1_1		USART1_CK USART1_CK_1 USART1_RX_2		MCO		I2S3_MCK					
PA9		TIM1_CH2 TIM1_CH2_1		USART1_TX USART1_RTS_2	OTG_FS_VBUS			I2S3_SD			DVP_D0		
PA10		TIM1_CH3 TIM1_CH3_1		USART1_RX USART1_CK_2	OTG_FS_ID						DVP_D1		
PA11		TIM1_CH4 TIM1_CH4_1		USART1_CTS USART1_CTS_1	OTG_FS_DM								CAN1_RX
PA12		TIM1_ETR TIM1_ETR_1 TIM10_CH1N		USART1_RTS USART1_RTS_1	OTG_FS_DP								CAN1_TX
PA13		TIM8_CH1N_1 TIM10_CH2N		USART3_TX_2		SWDIO							
PA14		TIM8_CH2N_1 TIM10_CH3N		UART8_TX_1 USART3_RX_2		SWCLK							
PA15		TIM8_CH3N_1	TIM2_CH1_1 TIM2_ETR_1 TIM2_CH1_3 TIM2_ETR_3	UART8_RX_1				SPI1_NSS_1 SPI3_MOSI SPI3_NSS I2S3_WS					
PB0	ADC_IN8	TIM1_CH2N_1 TIM8_CH2N TIM9_CH1N_1	TIM3_CH3 TIM3_CH3_2	UART4_TX_1					ETH_MII_RXD2 ETH_RGMII_TXD3			OPA1_CH1P	
PB1	ADC_IN9	TIM1_CH3N_1 TIM8_CH3N TIM9_CH2N_1	TIM3_CH4 TIM3_CH4_2	UART4_RX_1					ETH_MII_RXD3 ETH_RGMII_125IN			OPA4_CH0N	
PB2		TIM9_CH3N_1				BOOT1						OPA3_CH0N	
PB3		TIM10_CH1_1	TIM2_CH2_1 TIM2_CH2_3					SPI1_SCK_1 SPI3_SCK I2S3_CK			DVP_D5		

Alternate / Pin	ADC DAC	TIM1 8/9/10	TIM2 3/4/5	UART USART	USB	SYS	I2C	SPI I2S	ETH	FSMC SDIO	DVP	OPA	CAN
PB4		TIM10_CH2_1	TIM3_CH1_2	UART5_TX_1				SPI1_MISO_1 SPI3_MISO					
PB5		TIM10_CH3_1	TIM3_CH2_2	UART5_RX_1			I2C1_SMBA	SPI1_MOSI_1 SPI3_MOSI I2S3_SD	ETH_MII_PPS_OUT ETH_RMII_PPS_OUT				CAN2_RX_1
PB6		TIM8_CH1_1	TIM4_CH1	USART1_TX_1	USBFS_DM USBHS_DM		I2C1_SCL				DVP_D5		CAN2_TX_1
PB7		TIM8_CH2_1	TIM4_CH2	USART1_RX_1	USBFS_DP USBHS_DP		I2C1_SDA			FSMC_NADV			
PB8		TIM8_CH3_1 TIM10_CH1	TIM4_CH3	UART6_TX_1			I2C1_SCL_1		ETH_MII_TXD3	SDIO_D4	DVP_D6		CAN1_RX_2
PB9		TIM8_BKIN_1 TIM10_CH2	TIM4_CH4	UART6_RX_1			I2C1_SDA_1			SDIO_D5	DVP_D7		CAN1_TX_2
PB10		TIM10_BKIN_1	TIM2_CH3_2 TIM2_CH3_3	USART3_TX			I2C2_SCL		ETH_MII_RX_ER			OPA2_CH0N	
PB11		TIM10_ETR_1	TIM2_CH4_2 TIM2_CH4_3	USART3_RX			I2C2_SDA		ETH_MII_TX_EN ETH_RMII_TX_EN			OPA1_CH0N	
PB12		TIM1_BKIN		USART3_CK			I2C2_SMBA	SPI2_NSS I2S2_WS	ETH_MII_TXD0 ETH_RMII_TXD0 ETH_RGMII_MDC			OPA4_CH0P	CAN2_RX
PB13		TIM1_CH1N		USART3_CTS USART3_CTS_1				SPI2_SCK I2S2_CK	ETH_MII_TXD1 ETH_RMII_TXD1 ETH_RGMII_MDIO			OPA3_CH0P	CAN2_TX
PB14		TIM1_CH2N		USART3_RTS USART3_RTS_1				SPI2_MISO		SDIO_D0		OPA2_CH0P	
PB15		TIM1_CH3N		USART1_TX_2				SPI2_MOSI I2S2_SD		SDIO_D1		OPA1_CH0P	
PC0	ADC_IN10	TIM9_CH1N		UART6_TX					ETH_RGMII_RXC				
PC1	ADC_IN11	TIM9_CH2N		UART6_RX					ETH_MII_MDC ETH_RMII_MDC ETH_RGMII_RXCTL				
PC2	ADC_IN12	TIM9_CH3N		UART7_TX					ETH_MII_TXD2 ETH_RGMII_RXD0			OPA3_CH1N	
PC3	ADC_IN13	TIM10_CH3		UART7_RX					ETH_MII_TX_CLK ETH_RGMII_RXD1			OPA4_CH1N	
PC4	ADC_IN14	TIM9_CH4		USART1_CTS_3 UART8_TX					ETH_MII_RXD0 ETH_RMII_RXD0 ETH_RGMII_TXD1			OPA4_CH1P	
PC5	ADC_IN15	TIM9_BKIN		USART1_RTS_3 UART8_RX					ETH_MII_RXD1 ETH_RMII_RXD1 ETH_RGMII_TXD2			OPA3_CH1P	
PC6		TIM8_CH1	TIM3_CH1_3					I2S2_MCK	ETH_RXP	SDIO_D6			
PC7		TIM8_CH2	TIM3_CH2_3					I2S3_MCK	ETH_RXN	SDIO_D7			
PC8		TIM8_CH3	TIM3_CH3_3						ETH_TXP	SDIO_D0	DVP_D2		
PC9		TIM8_CH4	TIM3_CH4_3						ETH_TXN	SDIO_D1	DVP_D3		
PC10		TIM10_ETR		USART3_TX_1 UART4_TX				SPI3_SCK_1 I2S3_CK_1		SDIO_D2	DVP_D8		
PC11		TIM10_CH4		USART3_RX_1 UART4_RX				SPI3_MISO_1		SDIO_D3	DVP_D4		
PC12		TIM10_BKIN		USART3_CK_1 UART5_TX				SPI3_MOSI_1 I2S3_SD_1		SDIO_CK	DVP_D9		
PC13		TIM8_CH4_1				TAMPER-RTC							
PC14		TIM9_CH4_1				OSC32_IN							
PC15		TIM10_CH4_1				OSC32_OUT							
PD0		TIM10_ETR_2 TIM10_ETR_3				OSC_IN				FSMC_D2			CAN1_RX_3
PD1		TIM10_CH1_2 TIM10_CH1_3				OSC_OUT				FSMC_D3			CAN1_TX_3
PD2			TIM3_ETR TIM3_ETR_2	UART5_RX						SDIO_CMD FSMC_NADV	DVP_D11		

Alternate / Pin	ADC DAC	TIM1 8/9/10	TIM2 3/4/5	UART USART	USB	SYS	I2C	SPI I2S	ETH	FSMC SDIO	DVP	OPA	CAN
			TIM3_ETR_3										
PD3		TIM10_CH2_2 TIM10_CH2_3		USART2_CTS_1						FSMC_CLK			
PD4				USART2_RTS_1						FSMC_NOE			
PD5		TIM10_CH3_2 TIM10_CH3_3		USART2_TX_1						FSMC_NWE			
PD6				USART2_RX_1						FSMC_NWAIT	DVP_D10		
PD7		TIM10_CH4_2 TIM10_CH4_3		USART2_CK_1						FSMC_NE1 FSMC_NCE2			
PD8		TIM9_CH1N_2 TIM9_CH1N_3		USART3_TX_3					ETH_MII_RX_DV_1 ETH_RMII_CRS_DV_1	FSMC_D13			
PD9		TIM9_CH1_2 TIM9_ETR_2 TIM9_CH1_3 TIM9_ETR_3		USART3_RX_3					ETH_MII_RXD0_1 ETH_RMII_RXD0_1	FSMC_D14			
PD10		TIM9_CH2N_2 TIM9_CH2N_3		USART3_CK_3 USART3_CK_2					ETH_MII_RXD1_1 ETH_RMII_RXD1_1	FSMC_D15			
PD11		TIM9_CH2_2 TIM9_CH2_3		USART3_CTS_3 USART3_CTS_2					ETH_MII_RXD2_1	FSMC_A16			
PD12		TIM9_CH3N_2 TIM9_CH3N_3	TIM4_CH1_1	USART3_RTS_3 USART3_RTS_2					ETH_MII_RXD3	FSMC_A17			
PD13		TIM9_CH3_2 TIM9_CH3_3	TIM4_CH2_1							FSMC_A18			
PD14		TIM9_BKIN_2 TIM9_BKIN_3	TIM4_CH3_1							FSMC_D0			
PD15		TIM9_CH4_2 TIM9_CH4_3	TIM4_CH4_1							FSMC_D1			
PE0			TIM4_ETR TIM4_ETR_1	UART4_TX_2 UART4_TX_3						FSMC_NBL0			
PE1				UART4_RX_2 UART4_RX_3						FSMC_NBL1			
PE2		TIM10_BKIN_2 TIM10_BKIN_3								FSMC_A23			
PE3		TIM10_CH1N_2 TIM10_CH1N_3								FSMC_A19			
PE4		TIM10_CH2N_2 TIM10_CH2N_3								FSMC_A20			
PE5		TIM10_CH3N_2 TIM10_CH3N_3								FSMC_A21			
PE6										FSMC_A22			
PE7		TIM1_ETR_3								FSMC_D4		OPA3_OUT1	
PE8		TIM1_CH1N_3		UART5_TX_2 UART5_TX_3						FSMC_D5		OPA4_OUT1	
PE9		TIM1_CH1_3		UART5_RX_2 UART5_RX_3						FSMC_D6			
PE10		TIM1_CH2N_3		UART6_TX_2 UART6_TX_3						FSMC_D7			
PE11		TIM1_CH2_3		UART6_RX_2 UART6_RX_3						FSMC_D8			
PE12		TIM1_CH3N_3		UART7_TX_2 UART7_TX_3						FSMC_D9			
PE13		TIM1_CH3_3		UART7_RX_2 UART7_RX_3						FSMC_D10			
PE14		TIM1_CH4_3		UART8_TX_2 UART8_TX_3						FSMC_D11		OPA2_OUT1	
PE15		TIM1_BKIN_3		UART8_RX_2 UART8_RX_3						FSMC_D12		OPA1_OUT1	

Chapter 4 Electrical Characteristics

4.1 Test Conditions

Unless otherwise specified and marked, all voltages are referenced to V_{SS}.

All minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and clock frequency.

The typical values of CH32V303/305/307 are based on the ambient temperature of 25°C and V_{DD} = 3.3V for design guidance.

The typical value of CH32V317 is based on the ambient temperature of 25°C, VDD = 3.3V and V_{DD_ETH} = 3.3V for design guidance.

The data based on comprehensive evaluation, design simulation or technology characteristics are not tested in production. On the basis of comprehensive evaluation, the minimum and maximum values refer to sample tests. Unless otherwise specified that is tested, the characteristic parameters are guaranteed by comprehensive evaluation or design.

Power supply scheme:

Figure 4-1-1 CH32V303/305/307 typical circuit for conventional power supply

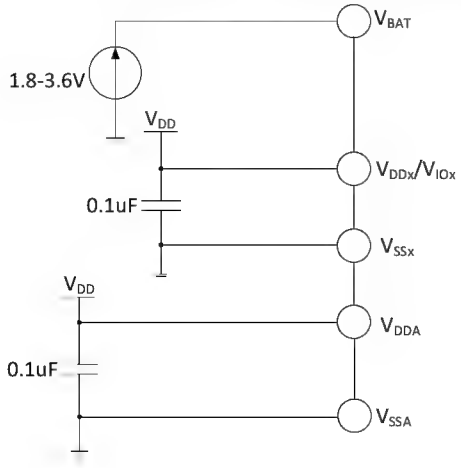
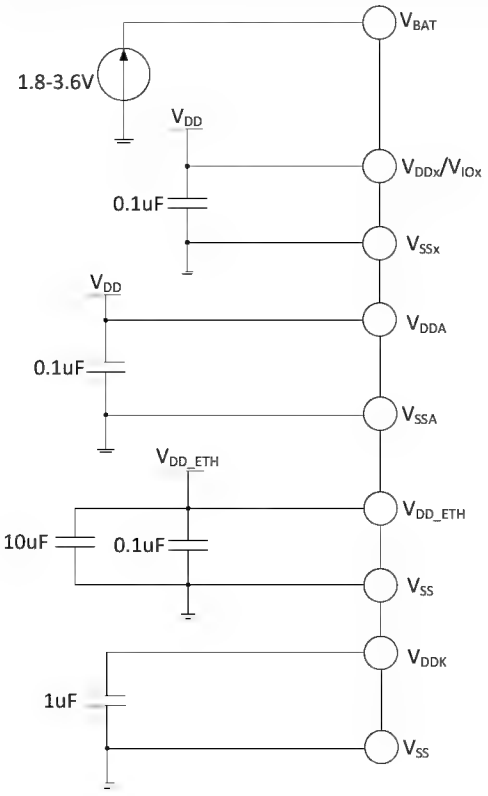


Figure 4-1-2 CH32V317 typical circuit for conventional power supply



4.2 Absolute Maximum Ratings

Stresses at or above the absolute maximum ratings listed in the table below may cause permanent damage to the device.

Table 4-1 Absolute maximum ratings

Symbol	Description		Min.	Max.	Unit
T_A	Ambient temperature during operation		-40	85	℃
T_S	Ambient temperature during storage		-40	125	℃
V_{DD}-V_{SS}	External main supply voltage (includingV_{DDA} and V_{DD})		-0.3	4.0	V
$V_{I/O}$-V_{SS}	I/O supply voltage		-0.3	4.0	V
V_{DD_ETH}-V_{SS}	Internal 10/100M Ethernet PHY supply voltage	CH32V317	-0.3	4.0	V
V_{DDK}	Voltage at decoupling end of internal power supply LDO	CH32V317	-0.2	1.5	V
V_{IN}	Input voltage on the FT (5V tolerance) pin		V_{SS}-0.3	5.5	V
	10/100M Ethernet PHY differential pin	V_{SS}-0. 3	V_{DD_ETH}+0.3	V	V
	Input voltage on PHY pin of USB and 10M Ethernet		V_{SS}-0.3	V_{DD}+0.3	V
	Input voltage on other pins		V_{SS}-0.3	V_{IO}+0.3	V
$\|\triangle V_{DD_x}\|$	Variations between different main power supply pins			50	mV
$\|\triangle V_{I/O_x}\|$	Variations between different I/O power supply pins			50	mV
$\|\triangle V_{SS_x}\|$	Variations between different ground pins			50	mV
$V_{ESD(HBM)}$	Electrostatic discharge voltage (HBM, non-contact)		4K		V
	USB pins (PA11, PA12)		3K		V

I_{VDD}	Total current into $V_{DD}/V_{DDA}/V_{IO}$ power lines (source)		150	mA
I_{Vss}	Total current out of V_{SS} ground lines (sink)		150	
$I_{I/O}$	Sink current on any I/O and control pin		25	
	Source current on any I/O and control pin		-25	
$I_{INJ(PIN)}$	Injected current on NRST pin		+/-5	
	Injected current on HSE's OSC_IN pin and LSE's OSC_IN pin		+/-5	
	Injected current on other pins		+/-5	
$\sum I_{INJ(PIN)}$	Total injected current on all I/Os and control pins		+/-25	

4.3 Electrical Characteristics

4.3.1 Operating Conditions

Table 4-2 General operating conditions

Symbol	Parameter	Condition	Min.	Max.	Unit
F_{HCLK}	Internal HB clock frequency			144	MHz
F_{PCLK1}	Internal PB1 clock frequency			144	MHz
F_{PCLK2}	Internal PB2 clock frequency			144	MHz
V_{DD}	Standard operating voltage	USB or ETH not used.	2.4	3.6	V
		Use USB or ETH	3.0	3.6	
V_{IO}	Output voltage on most I/O pins	$V_{I/O}$ cannot be more than V_{DD}	2.4	3.6	V
V_{DDA}	Analog operating voltage (ADC is not used)	V_{DDA} must be the same as $V_{I/O}$, V_{REF+} cannot be higher than V_{DDA}, V_{REF-} is equal to V_{SS}.	2.4	3.6	V
	Analog operating voltage (ADC is used)				
V_{DD_ETH}	Internal 10/100M Ethernet PHY power supply voltage (CH32V317)		3.2	3.45	V
V_{BAT}(1)	Backup operating voltage	Cannot be more than V_{DD}	1.8	3.6	V
T_A	Ambient temperature		-40	85	℃
T_J	Junction temperature range		-40	105	℃

Note: 1. The connection line from the battery to V_{BAT} should be as short as possible.

2. For the chip with bit VLEVEL = 1, V_{DD}, V_{IO} and V_{DDA} support the minimum power supply voltage of 2.4 V; For the chip with bit V_{LEVEL} = 0, the minimum power supply voltage supported by V_{DD}, V_{IO} and V_{DDA} is 1.8V; When ADC, DAC and OPA peripherals are used, the minimum supply voltage supported by V_{DD}, V_{IO} and V_{DDA} is still 2.4V.

Table 4-3 Power-on and power-down conditions

Symbol	Parameter	Condition	Min.	Max.	Unit
t_{VDD}	V_{DD} rise time rate		0	∞	us/V
	V_{DD} fall time rate		20	∞	

4.3.2 Built-in Reset and Power Control Block Characteristics

Table 4-4-1 Reset and voltage monitor (For chips with bit VLEVEL = 1)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{PVD}(1)	Level selection of programmable voltage detector(2)	PLS[2:0] = 000 (rising edge)		2.39		V
		PLS[2:0] = 000 (falling edge)		2.31		V
		PLS[2:0] = 001 (rising edge)		2.56		V
		PLS[2:0] = 001 (falling edge)		2.48		V
		PLS[2:0] = 010 (rising edge)		2.65		V
		PLS[2:0] = 010 (falling edge)		2.57		V
		PLS[2:0] = 011 (rising edge)		2.78		V
		PLS[2:0] = 011 (falling edge)		2.69		V
		PLS[2:0] = 100 (rising edge)		2.89		V
		PLS[2:0] = 100 (falling edge)		2.81		V
		PLS[2:0] = 101 (rising edge)		3.05		V
		PLS[2:0] = 101 (falling edge)		2.96		V
		PLS[2:0] = 110 (rising edge)		3.17		V
		PLS[2:0] = 110 (falling edge)		3.08		V
		PLS[2:0] = 111 (rising edge)		3.31		V
		PLS[2:0] = 111 (falling edge)		3.21		V
$V_{PVDhyst}$	PVD hysteresis			0.08		V
$V_{POR/PDR}$	Power-on/power-down reset threshold	Rising edge		2.2		V
		Falling edge		2.2		V
$V_{PDRhyst}$	PDR hysteresis			20		mV
$t_{RSTTEMPO}$	Power on reset		24	28	30	mS
	Other resets		8	10	30	

Note: 1. Normal temperature test value.

2. For CH32V317 chip, PLS[2:0] is recommended to be configured as 110 or 111.

Table 4-4-2 Reset and voltage monitor (For chips with bit VLEVEL = 0)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{PVD} (1)	Level selection of programmable voltage detector	PLS[2:0] = 000 (rising edge)		2.19		V
		PLS[2:0] = 000 (falling edge)		2.13		V
		PLS[2:0] = 001 (rising edge)		2.33		V
		PLS[2:0] = 001 (falling edge)		2.25		V
		PLS[2:0] = 010 (rising edge)		2.39		V
		PLS[2:0] = 010 (falling edge)		2.32		V
		PLS[2:0] = 011 (rising edge)		2.48		V
		PLS[2:0] = 011 (falling edge)		2.42		V
		PLS[2:0] = 100 (rising edge)		2.57		V
		PLS[2:0] = 100 (falling edge)		2.51		V
		PLS[2:0] = 101 (rising edge)		2.69		V
		PLS[2:0] = 101 (falling edge)		2.61		V
		PLS[2:0] = 110 (rising edge)		2.78		V

		PLS[2:0] = 110 (falling edge)		2.69		V
		PLS[2:0] = 111 (rising edge)		2.88		V
		PLS[2:0] = 111 (falling edge)		2.79		V
$V_{PVDhyst}$	PVD hysteresis			0.08		V
$V_{POR/PDR}$	Power-on/power-down reset threshold	Rising edge		1.59		V
		Falling edge		1.57		V
$V_{PDRhyst}$	PDR hysteresis			20		mV
$t_{RSTTEMPO}$	Power on reset		16	28	30	mS
	Other resets		2	10	30	

Note: 1. Normal temperature test value.

4.3.3 Built-in Reference Voltage

Table 4-5 Embedded reference voltage

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{REFINT}	Internal reference voltage	T_A = -40°C~85°C	1.17	1.2	1.23	V
$T_{S_vrefint}$	ADC sampling time when reading the internal reference voltage				17.1	us

4.3.4 Supply Current Characteristics

Current consumption is a comprehensive index of a variety of parameters and factors. These parameters and factors include operating voltage, ambient temperature, I/O pin load, the software configuration of the product, the operating frequency, flip rate of the I/O pin, the location of the program in memory and the executed code, etc. The current consumption measurement method is as follows:

Figure 4-2-1 CH32V303/305/307 current consumption measurement

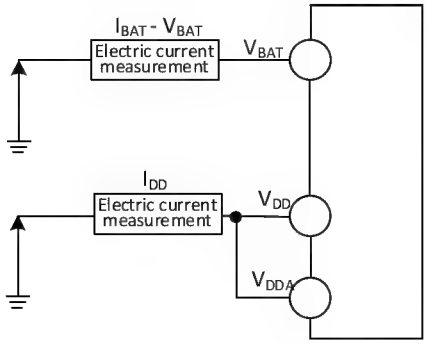
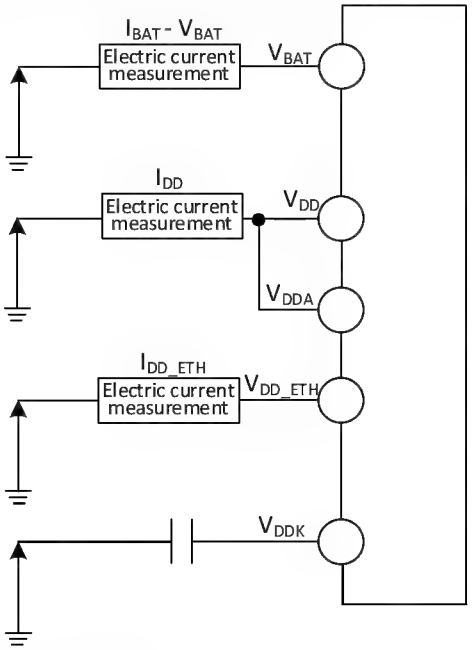


Figure 4-2-2 CH32V317 current consumption measurement



CH32V303/305/307 is in the following conditions:

Under normal temperature conditions and when V_{DD} = 3.3V, all I/O ports are configured with pull-down inputs, only one of HSE and HIS is enabled, HSE=8M, HIS=8M (calibrated), $F_{PLCK1}=F_{HCLK}/2$, $F_{PLCK2}=F_{HCLK}$, PLL is enabled when FHCLK>8MHz. Enable or disable the power consumption of all peripheral clocks.

CH32V317 is in the following conditions:

Under normal temperature conditions and when V_{DD} = 3.3V, V_{DD_ETH} = 3.3V all I/O ports are configured with pull-down inputs, only one of HSE and HIS is enabled, HSE=8M, HIS=8M (calibrated), $F_{PLCK1}=F_{HCLK}/2$, $F_{PLCK2}=F_{HCLK}$, PLL is enabled when FHCLK>8MHz. Enable or disable the power consumption of all peripheral clocks.

Table 4-6 Typical current consumption in Run mode, the data processing code runs from the internal Flash

Symbol	Parameter	Condition		Typ.		Unit
				All peripherals enabled	All peripherals disabled	
I_{DD}(1)	Supply current in Run mode	External clock	F_{HCLK} = 144MHz	22.4	12.4	mA
			F_{HCLK} = 72MHz	11.5	6.5	
			F_{HCLK} = 48MHz	8.0	4.6	
			F_{HCLK} = 36MHz	6.4	3.8	
			F_{HCLK} = 24MHz	4.4	2.7	
			F_{HCLK} = 16MHz	3.5	2.3	
			F_{HCLK} = 8MHz	1.8	1.3	
			F_{HCLK} = 4MHz	1.3	1.0	
			F_{HCLK} = 500kHz	0.8	0.7	
		Runs on the high-speed internal RC oscillator (HSI).	F_{HCLK} = 144MHz	22.1	12.2	
			F_{HCLK} = 72MHz	11.3	6.3	
			F_{HCLK} = 48MHz	7.7	4.3	

		Uses HB prescaler to reduce the frequency.	F_{HCLK} = 36MHz	5.8	3.3	
			F_{HCLK} = 24MHz	4.1	2.4	
			F_{HCLK} = 16MHz	3.0	1.8	
			F_{HCLK} = 8MHz	1.5	1.0	
			F_{HCLK} = 4MHz	1.0	0.7	
			F_{HCLK} = 500kHz	0.4	0.4	

Note: The above are measured parameters.

Table 4-7 Typical current consumption in Sleep mode, data processing code runs from internal Flash or SRAM

Symbol	Parameter	Condition		Typ.		Unit
				All peripherals enabled	All peripherals disabled	
I_{DD}(1)	Supply current in Sleep mode (In this case, peripheral power supply and clock are maintained)	External clock	F_{HCLK} = 144MHz	13.7	3.8	mA
			F_{HCLK} = 72MHz	7.2	2.3	
			F_{HCLK} = 48MHz	5.1	1.8	
			F_{HCLK} = 36MHz	4.0	1.5	
			F_{HCLK} = 24MHz	2.9	1.3	
			F_{HCLK} = 16MHz	2.2	1.1	
			F_{HCLK} = 8MHz	1.4	0.8	
			F_{HCLK} = 4MHz	1.0	0.8	
			F_{HCLK} = 500kHz	0.7	0.7	
		Runs on the high-speed internal RC oscillator (HSI). Uses HB prescaler to reduce the frequency.	F_{HCLK} = 144MHz	13.4	3.5	
			F_{HCLK} = 72MHz	6.9	1.9	
			F_{HCLK} = 48MHz	4.7	1.4	
			F_{HCLK} = 36MHz	3.6	1.2	
			F_{HCLK} = 24MHz	2.6	0.9	
			F_{HCLK} = 16MHz	1.9	0.7	
			F_{HCLK} = 8MHz	1.0	0.5	
			F_{HCLK} = 4MHz	0.7	0.4	
			F_{HCLK} = 500kHz	0.4	0.3	

Note: The above are measured parameters.

Table 4-8 Typical current consumption in Stop and Standby mode

Symbol	Parameter	Condition	Typ.	Unit
I_{DD}(1)	Supply current in Stop mode	Voltage regulator in Run mode, low-speed and high-speed internal RC oscillators and external oscillators off (no independent watchdog)	110	uA
		Voltage regulator in low-power mode, low-speed and high-speed internal RC oscillators and external oscillators off (no independent watchdog, PVD off), RAM enters low-power mode	30	

	Supply current in Standby mode	Low-speed internal RC oscillator and independent watchdog on, all RAM not powered	1.8	
		Low-speed internal RC oscillator on, independent watchdog off, all RAM not powered	1.8	
		LSI/LSE/RTC/IWDG off, 32K_RAM powered and in low-power mode	2.5	
		LSI/LSE/RTC/IWDG off, 2K_RAM powered and in low-power mode	1.2	
		LSI/LSE/RTC/IWDG off, all RAM not powered	1	
I_{DD_VBAT}(1)	Backup domain supply current (Remove V_{DD} and V_{DDA}, only powered by V_{BAT}	Low-speed external oscillator and RTC on	1.8	

Note: The above are measured parameters.

The CH32V317 chip has a built-in 10/100Mbps Ethernet PHY physical layer transceiver, and the current consumption of this module is shown in Table 4-9 below.

Table 4-8 Current consumption of 10/100Mbps Ethernet PHY module (only for CH32V317 chip)

Symbol	Parameter	Condition	Typ.	Unit
$I_{DD_10/100M_PHY}$	Supply current in transmission state	The link of 100BASE-TX path is successful and there are packets on the transceiver channel.	60.4	mA
		The link of 10BASE-TX path is successful and there are packets on the transceiver channel.	34.2	
	Supply current in idle state	The link of 100BASE-TX path is successful and there are no data packets on the transceiver channel.	61.4	
		The link of 10BASE-TX path is successful and there are no data packets on the transceiver channel.	28.1	
	Supply current in disconnected state	100BASE-TX and 10BASE-TX paths are not linked successfully and PHY is in auto-negotiation state.	38.4	
	Supply current in shutdown state	Only SMI interface in work state	0.2	

4.3.5 External Clock Source Characteristics

Table 4-10 From external high-speed clock

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit

F_{HSE_ext}	External clock frequency		3	8	25	MHz
V_{HSEH}(1)	OSC_IN input pin high level voltage		$0.8V_{I/O}$		$V_{I/O}$	V
V_{HSEL}(1)	OSC_IN input pin low-level voltage		0		$0.2V_{I/O}$	V
$C_{in(HSE)}$	OSC_IN input capacitance			5		pF
$DuCy_{HSE}$	Duty cycle			50		%
I_L	OSC_IN input leakage current				±1	uA

Note: 1. Failure to meet this condition may cause level recognition error.

Figure 4-3 External high-frequency clock source circuit

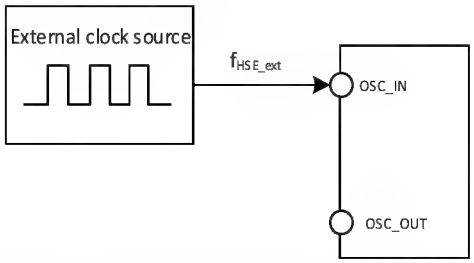


Table 4-11 From external low-speed clock

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{LSE_ext}	User external clock frequency			32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.8V_{DD}$		V_{DD}	V
V_{LSEL}	OSC32_IN input pin low voltage		0		$0.2V_{DD}$	V
$C_{in(LSE)}$	OSC32_IN input capacitance			5		pF
$DuCy_{(LSE)}$	Duty cycle			50		%
I_L	OSC32_IN input leakage current				±1	uA

Figure 4-4 External low-frequency clock source circuit

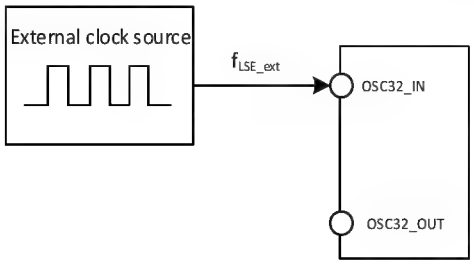


Table 4-12 High-speed external clock generated from a crystal/ceramic resonator

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{OSC_IN}	Resonator frequency		3	8	25	MHz
R_F	Feedback resistance			250		kΩ

C	Recommended load capacitance and corresponding crystal series impedance RS	R_S=60Ω(1)		30		pF
I_2	HSE drive current	V_{DD} = 3.3V， 20p load		0.53		mA
g_m	Oscillator transconductance	Startup		17		mA/V
$t_{SU(HSE)}$	Startup time	V_{DD} is stable, 8M crystal		1.5	4	ms

Note 1: It is recommended that the ESR of 25M crystal should not exceed 60 Ω, and it can be relaxed if it is lower than 25M.

2. For CH32V317 chip, the crystal frequency deviation is recommended to be within ±40ppm.

Circuit reference design and requirements:

The load capacitance of the crystal is subject to the recommendation of the crystal manufacturer, C_{L1}=C_{L2}.

Figure 4-5 Typical circuit of external 8M crystal

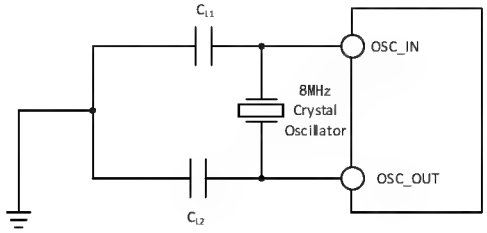


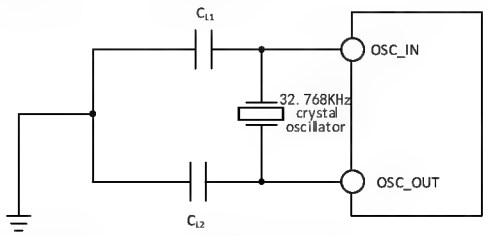
Table 4-13 Low-speed external clock generated by generated from a crystal/ceramic resonator (f_{LSE}=32.768kHz)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
R_F	Feedback resistance			5		MΩ
C	Recommended load capacitance and corresponding crystal serial impedance R_S	R_S<70kΩ			15	pF
i_2	LSE drive current	VDD = 3.3V		0.35		uA
g_m	Oscillator transconductance	Startup		25.3		uA/V
$t_{SU(LSE)}$	Startup time	VDD is stable		800		mS

Circuit reference design and requirements:

The load capacitance of the crystal is subject to the recommendation of the crystal manufacturer, C_{L1}=C_{L2}, generally 12pF is recommended.

Figure 4-6 Typical circuit of external 32.768K crystal



Note: The load capacitance C_L is calculated by the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$. C_{stray} is the capacitance of the pin and the PCB board or PCB-related capacitance. Its typical value is between 2pF and 7pF.

4.3.6 Internal Clock Source Characteristics

Table 4-14 Internal high-speed (HSI) RC oscillator characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{HSI}	Frequency (after calibration)			8		MHz
$DuCy_{HSI}$	Duty cycle		45	50	55	%
ACC_{HSI}	Accuracy of HSI oscillator (after calibration)	TA = 0°C~70°C	-1.8		1.8	%
		TA = -40°C~85°C	-3.0		2.5	%
$t_{SU(HSI)}$	HSI oscillator startup stabilization time				8	us
$I_{DD(HSI)}$	HSI oscillator power consumption		120	180	270	uA

Note: 1. Set register RCC_CTLR HSION 1, waiting for HSIRDY to set 1.

Table 4-15 Internal low-speed (LSI) RC oscillator characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{LSI}	Frequency		25	39	60	kHz
$DuCy_{LSI}$	Duty cycle		45	50	55	%
$t_{SU(LSI)}$	LSI oscillator startup stabilization time	LSE on		230		us
		LSE off		5		ms
$I_{DD(LSI)}$	LSI oscillator power consumption			0.6		uA

4.3.7 PLL Characteristics

Table 4-16 PLL characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{PLL_IN}	PLL input clock		3	8	25	MHz
	PLL input clock duty cycle		40		60	%
F_{PLL_OUT}	PLL multiplier output clock		18		144(1)	MHz
t_{LOCK}	PLL lock time			80	200	us

Note 1: The frequency multiplier must be selected to meet the PLL output frequency range.

Table 4-17 PLL2 and PLL3 characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{PLL_IN}	PLL input clock		3		25	MHz
	PLL input clock duty cycle1		40		60	%
F_{PLL_OUT}	PLL multiplier output clock		30		75(1)	MHz
F_{VCO}	VCO output clock		60		150	MHz
t_{LOCK1}	PLL lock time			80	200	us

Note 1: The frequency multiplier must be selected to meet the PLL output frequency range.

4.3.8 Wakeup Time from Low-power Mode

Table 4-18 Wakeup time from low-power mode(1)

Symbol	Parameter	Condition	Typ.	Unit

$t_{wusleep}$	Wakeup from Sleep mode	Wake up using HSI RC clock	2.4	us
t_{wustop}	Wakeup from Stop mode (voltage regulator is in Run mode)	Wake on HSI RC clock	23.1	us
	Wakeup from Stop mode (voltage regulator is in low-power mode)	Voltage regulator wake-up time from low-power mode + HSI RC clock wake up	76.7	us
$t_{WUSTDBY}$	Wakeup from Standby mode	LDO stabilization time + HSI RC clock wake up + code load time(2) (take 256K as example)	8.9	ms

Note: 1. The above parameters are measured parameters.

2. The code load time is calculated based on the current zero-wait area capacity configured by the chip and the size of the loading configuration clock.

4.3.9 Memory Characteristics

Table 4-19 Flash memory characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{prog}	Programming frequency(1)	T_A = -40°C～85°C			60	MHz
t_{prog_page}	Page (256 bytes) programming time	T_A = -40°C～85°C		2	2.5	ms
t_{erase_page}	Page (256 bytes) erase time	T_A = -40°C～85°C		16	20	ms
t_{erase_sec}	Sector (4K bytes) erase time	T_A = -40°C～85°C		16	20	ms
V_{prog}	Programming voltage		2.4		3.6	V

Note: 1. For the programming frequency of flash, read operation, program operation and erase operation are included. The clock is from HCLK.

Table 4-20 Flash memory endurance and data retention

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
N_{END}	Endurance	T_A = 25°C	10K	80K(1)		times
t_{RET}	Data retention		20			year

Note: The endurance parameter is actual measured, which is not guaranteed.

4.3.10 I/O Port Characteristics

Table 4-21 General-purpose I/O static characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IH}	Standard I/O pin, input high-level voltage		0.41*(V_{IO}-1.8)+1.3		V_{IO}+0.3	V
	FT I/O pin, input high level voltage		0.42*(V_{IO}-1.8)+1		5.5	V
V_{IL}	Standard I/O pin, input low-level voltage		-0.3		0.28*(V_{IO}-1.8)+0.6	V
	FT I/O pin, input low-level voltage		-0.3		0.32*(V_{IO}-1.8)+0.55	V

V_{hys}	Standard I/O pin Schmitt trigger voltage hysteresis		150			mV
	FT I/O pin Schmitt trigger voltage hysteresis		90			
I_{lkg}	Input leakage current	Standard I/O port			1	uA
		FT I/O port			3	
R_{PU}	Pull-up equivalent resistance		30	40	50	kΩ
R_{PD}	Pull-down equivalent resistance		30	40	50	kΩ
$C_{I/O}$	I/O pin capacitance			5		pF

Output drive current characteristics

GPIO (General-Purpose Input/Output Port) can sink or output up to ±8mA current, and sink or output ±20mA current (not strictly to V_{OL}/V_{OH}). In user applications, the total driving current of all I/O pins cannot exceed the absolute maximum ratings given in Section 4.2:

Table 4-22 Output voltage characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit
V_{OL}	Output low level, 8 pins sink current	TTL port, I_{IO} = +8mA		0.4	V
V_{OH}	Output high level, 8 pins source current	2.7V< V_{DD} <3.6V	V_{DD}-0.4		
V_{OL}	Output low level, 8 pins sink current	CMOS port, I_{IO} = +8mA		0.4	V
V_{OH}	Output high level, 8 pins source current	2.7V< V_{DD} <3.6V	V_{DD}-0.4		
V_{OL}	Output low level, 8 pins sink current	I_{IO} = +20mA		1.0	V
V_{OH}	Output high level, 8 pins source current	2.7V< V_{DD} <3.6V	V_{DD}-1.2		
V_{OL}	Output low level, 8 pins sink current	I_{IO} = +6mA		0.4	V
V_{OH}	Output high level, 8 pins source current	2.4V< V_{DD} <2.7V	V_{DD}-0.6		

Note: In the above conditions, if multiple IO pins are driven at the same time, the total current cannot exceed the absolute maximum ratings given in Table 4.2. In addition, when multiple I/O pins are driven at the same time, the current on the power/ground point is very large, which will cause the voltage drop to make the internal I/O voltage not reach the power supply voltage in the table, resulting in the drive current being less than the nominal value.

Table 4-23 Input/output AC characteristics

MODEx[1:0] configuration	Symbol	Parameter	Condition	Min.	Max.	Unit
10 (2MHz)	$F_{max(IO)out}$	Maximum frequency	CL=50pF,V_{DD}=2.7-3.6V		2	MHz
	$t_{f(IO)out}$	Output high to low fall time	CL=50pF,V_{DD}=2.7-3.6V		125	ns
	$t_{r(IO)out}$	Output low to high rise time			125	ns
01 (10MHz)	$F_{max(IO)out}$	Maximum frequency	CL=50pF,V_{DD}=2.7-3.6V		10	MHz
	$t_{f(IO)out}$	Output high to low fall time	CL=50pF,V_{DD}=2.7-3.6V		25	ns
	$t_{r(IO)out}$	Output low to high rise time			25	ns
11 (50MHz)	$F_{max(IO)out}$	Maximum frequency	CL=30pF,V_{DD}=2.7-3.6V		50	MHz
			CL=50pF,V_{DD}=2.7-3.6V		30	MHz
	$t_{f(IO)out}$	Output high to low fall time	CL=30pF,V_{DD}=2.7-3.6V		5	ns

			CL=50pF,V_{DD}=2.7-3.6V		8	ns
	$t_{r(IO)out}$	Output low to high rise time	CL=30pF,V_{DD}=2.7-3.6V		5	ns
			CL=50pF,V_{DD}=2.7-3.6V		8	ns
	t_{EXTIpw}	The EXTI controller detects the pulse width of the external signal		10		ns

4.3.11 NRST Pin Characteristics

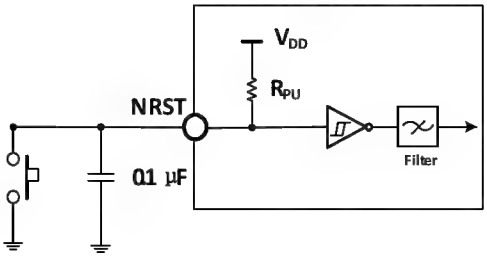
Table 4-24 External reset pin characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$V_{IL(NRST)}$	NRST input low-level voltage		-0.3		0.28*(V_{DD}-1.8)+0.6	V
$V_{IH(NRST)}$	NRST input high-level voltage		0.41*(V_{DD}-1.8)+1.3		V_{DD}+0.3	V
$V_{hys(NRST)}$	NRST Schmitt Trigger voltage hysteresis		150			mV
R_{PU}(1)	Pull-up equivalent resistance		30	40	50	kΩ
$V_{F(NRST)}$	NRST input filtered pulse width				100	ns
$V_{NF(NRST)}$	NRST input not filtered pulse width		300			ns

Note: 1. The pull-up resistor is a real resistor in series with a switchable PMOS implementation. The resistance of this PMOS switch is very small (approximately 10%).

Circuit reference design and requirements:

Figure 4-7 Typical circuit of external reset pin



4.3.12 TIM Timer Characteristics

Table 4-25 TIMx characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit
$t_{res(TIM)}$	Timer reference clock		1		$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72MHz	13.9		ns
F_{EXT}	Timer external clock frequency on CH1 to CH4		0	$f_{TIMxCLK}$/2	MHz
		$f_{TIMxCLK}$ = 72MHz	0	36	MHz
R_{esTIM}	Timer resolution			16	bit

$t_{COUNTER}$	16-bit counter clock cycle when the internal clock is selected		1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72MHz	0.0139	910	us
t_{MAX_COUNT}	Maximum possible count			65535	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72MHz		59.6	s

4.3.13 I2C Interface Characteristics

Figure 4-8 I2C bus timing diagram

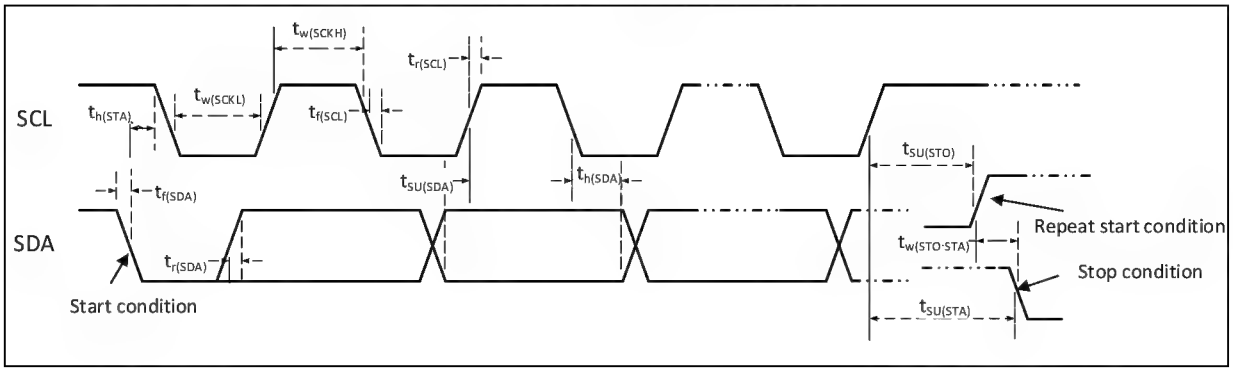


Table 4-26 I2C interface characteristics

Symbol	Parameter	Standard I2C		Fast I2C		Unit
		Min.	Max.	Min.	Max.	
$t_{w(SCKL)}$	SCL clock low time	4.7		1.2		us
$t_{w(SCKH)}$	SCL clock high time	4.0		0.6		us
$t_{SU(SDA)}$	SDA data setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0		0	900	ns
$t_{r(SDA)}/t_{r(SCL)}$	SDA and SCL rise time		1000	20		ns
$t_{f(SDA)}/t_{f(SCL)}$	SDA and SCL fall time		300			ns
$t_{h(STA)}$	Start condition hold time	4.0		0.6		us
$t_{SU(STA)}$	Repeated start condition setup time	4.7		0.6		us
$t_{SU(STO)}$	Stop condition setup time	4.0		0.6		us
$t_{w(STO:STA)}$	Time from stop condition to start condition (bus free)	4.7		1.2		us
C_b	Capacitive load for each bus		400		400	pF

4.3.14 SPI Interface Characteristics

Figure 4-9 SPI timing diagram in Master mode

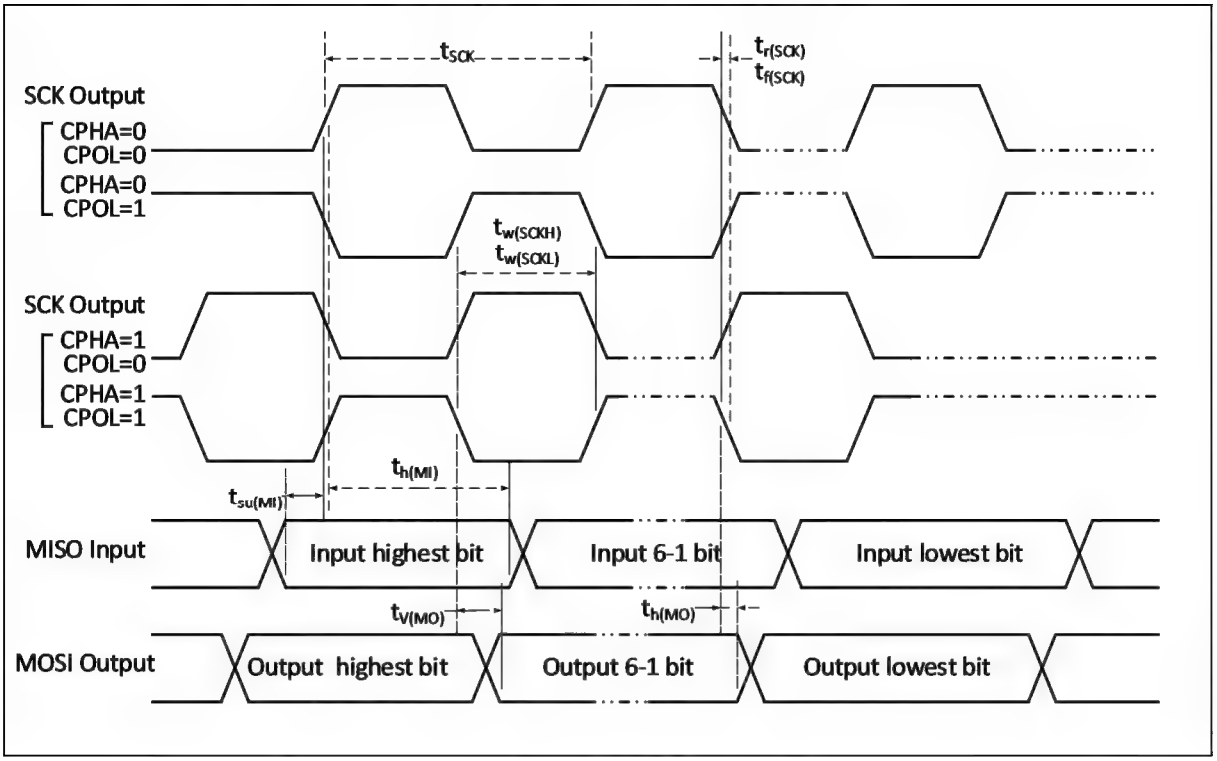


Figure 4-10 SPI timing diagram in Slave mode (CPHA=0)

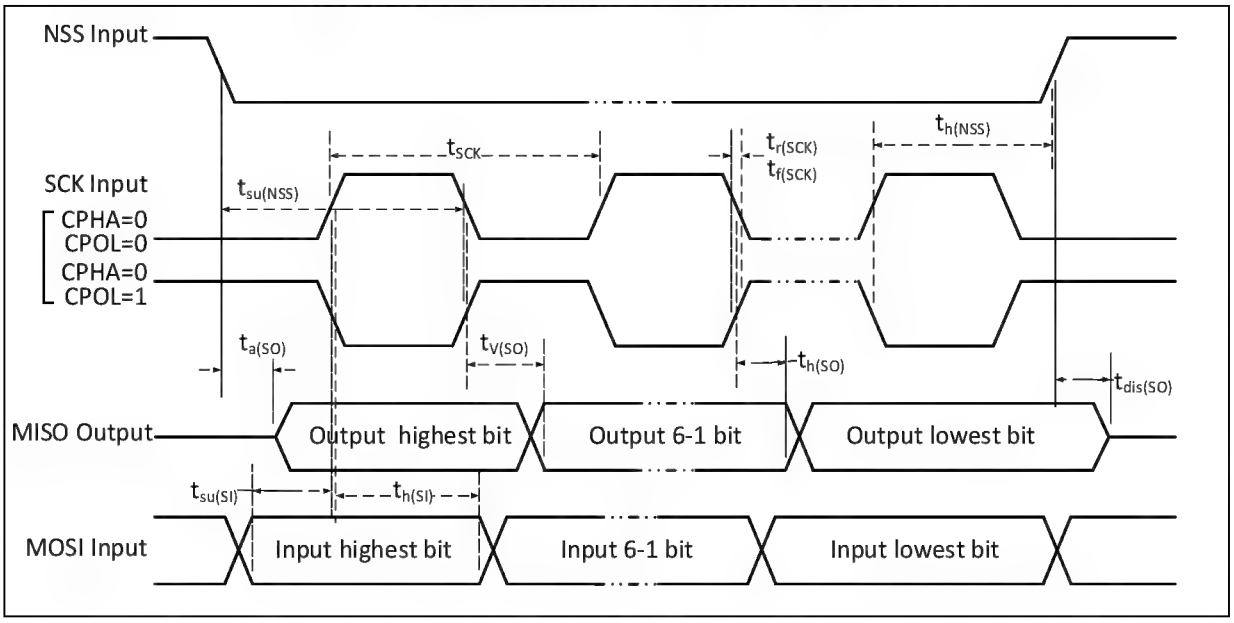


Figure 4-11 SPI timing diagram in Slave mode (CPHA=1)

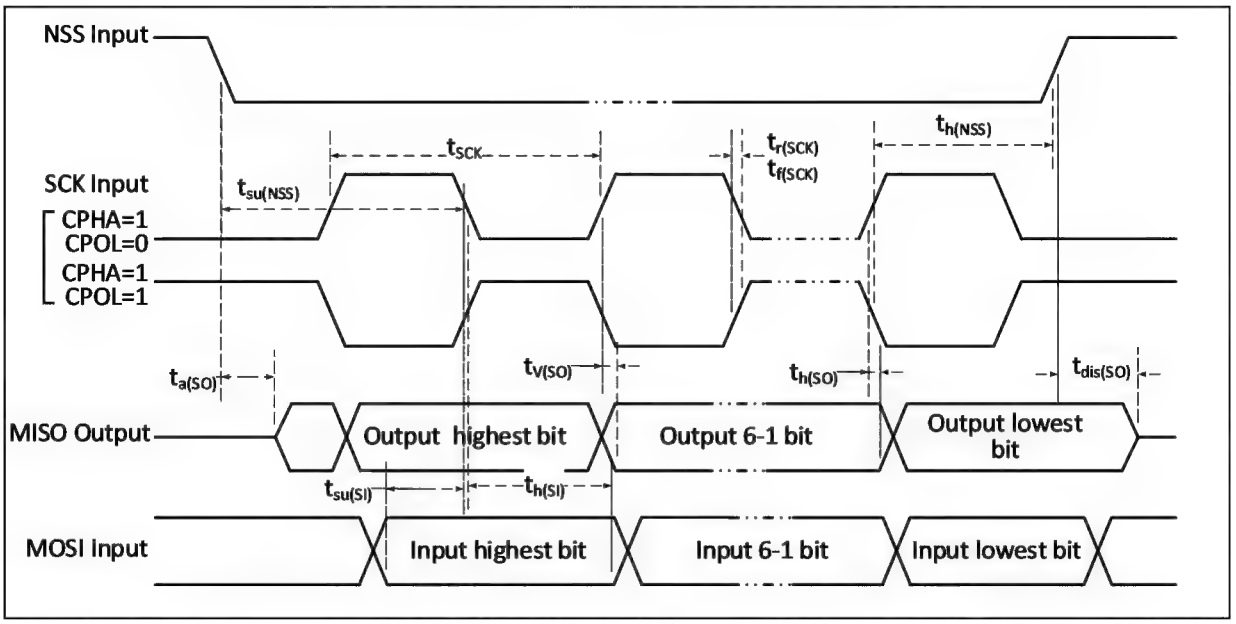


Table 4-27 SPI interface characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit
f_{SCK}/t_{SCK}	SPI clock frequency	Master mode		72	MHz
		Slave mode		72	MHz
$t_{r(SCK)}/t_{f(SCK)}$	SPI clock rise and fall time	Load capacitance:C = 30pF		20	ns
$t_{SU(NSS)}$	NSS setup time	Slave mode	$2t_{PCLK}$		ns
$t_{h(NSS)}$	NSS hold time	Slave mode	$2t_{PCLK}$		ns
$t_{w(SCKH)}/t_{w(SCKL)}$	SCK high and low time	Master mode, f_{PCLK} = 36MHz, Prescaler factor = 4	40	60	ns
$t_{SU(MI)}$	Data input setup time	Master mode	5		ns
$t_{SU(SI)}$		Slave mode	5		ns
$t_{h(MI)}$	Data input hold time	Master mode	5		ns
$t_{h(SI)}$		Slave mode	4		ns
$t_{a(SO)}$	Data output access time	Slave mode, f_{PCLK} = 20MHz	0	$1t_{PCLK}$	ns
$t_{dis(SO)}$	Data output disable time	Slave mode	0	10	ns
$t_{V(SO)}$	Data output valid time	Slave mode (After enable edge)		25	ns
$t_{V(MO)}$		Master mode (After enable edge)		5	ns
$t_{h(SO)}$	Data output hold time	Slave mode (After enable edge)	15		ns
$t_{h(MO)}$		Master mode (After enable edge)	0		ns

4.3.15 I2S Interface Characteristics

Figure 4-12 I2S master timing diagram (Philips protocol)

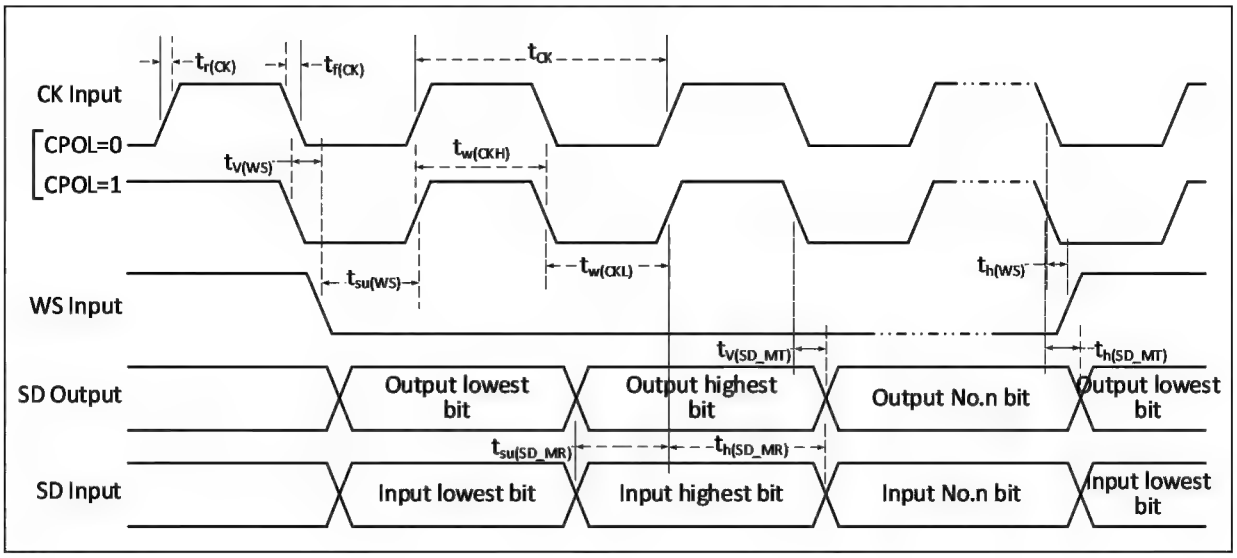


Figure 4-13 I2S slave timing diagram (Philips protocol)

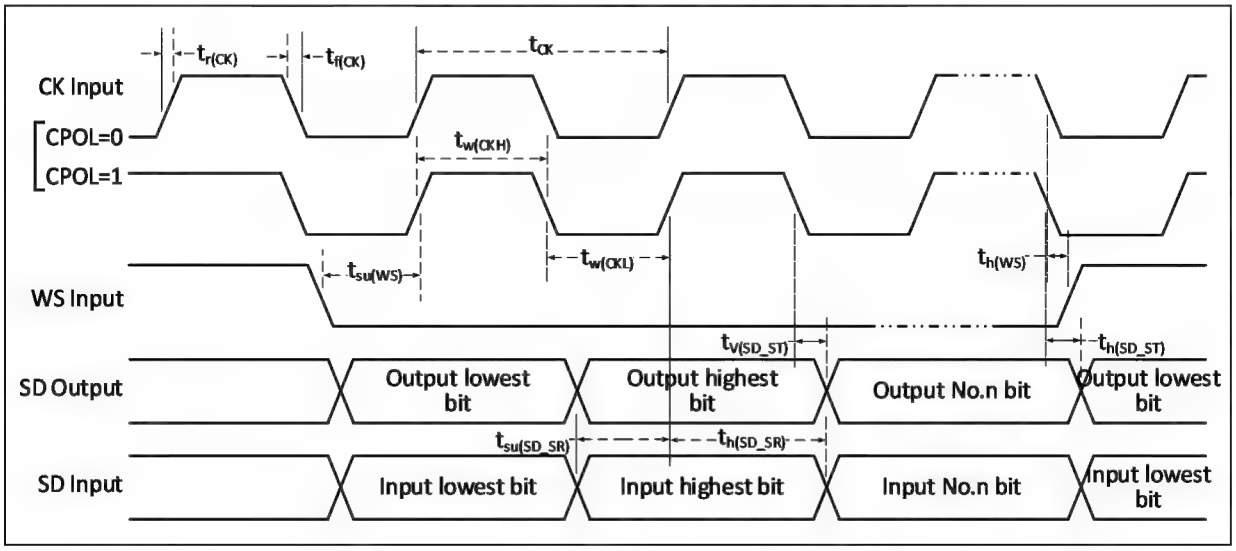


Table 4-28 I2S interface characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit
f_{CK}/t_{CK}	I²S clock frequency	Master mode		8	MHz
		Slave mode		8	MHz
$t_{r(CK)}/t_{f(CK)}$	I²S clock rise and fall time	Load capacitance: C = 30pF		20	ns
$t_{V(WS)}$	WS valid time	Master mode		5	ns
$t_{SU(WS)}$	WS setup time	Slave mode	10		ns
$t_{h(WS)}$	WS hold time	Master mode	0		ns
		Slave mode	0		ns
$t_{w(CKH)}/t_{w(CKL)}$	SCK high and low time	Master mode, f_{PCLK} = 36MHz,	40	60	%

		Prescaler factor =4			
$t_{SU(SD_MR)}$ $t_{SU(SD_SR)}$	Data input setup time	Master mode	8		ns
		Slave mode	8		ns
$t_{h(SD_MR)}$ $t_{h(SD_SR)}$	Data input hold time	Master mode	5		ns
		Slave mode	4		ns
$t_{h(SD_MT)}$	Data output hold time	Master mode (After enable edge)		5	ns
$t_{h(SD_ST)}$		Slave mode (After enable edge)		5	ns
$t_{V(SD_MT)}$	Data output valid time	Master mode (After enable edge)		5	ns
$t_{v(SD_ST)}$		Slave mode (After enable edge)		4	ns

4.3.16 USB Interface Characteristics

Table 4-29 USB characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit
V_{DD}	USB operating voltage		3.0	3.6	V
V_{SE}	Single-ended receiver threshold	V_{DD} = 3.3V	1.2	1.9	V
V_{OL}	Static output low level			0.3	V
V_{OH}	Static output high level		2.8	3.6	V
V_{HSSQ}	High-speed suppression information detection threshold		100	150	mV
V_{HSDSC}	High-speed disconnection detection threshold		500	625	mV
V_{HSOI}	High-speed idle level		-10	10	mV
V_{HSOH}	High-speed data high level		360	440	mV
V_{HSOL}	High-speed data low level		-10	10	mV

4.3.17 SD/MMC Interface Characteristics

Figure 4-14 SD high-speed timing diagram

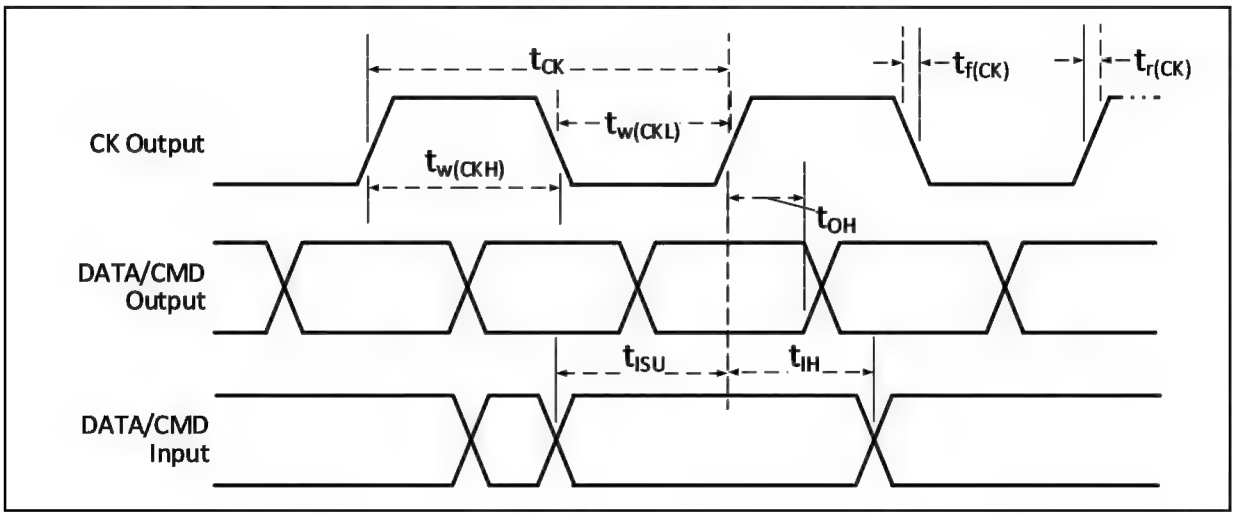


Figure 4-15 SD default timing diagram

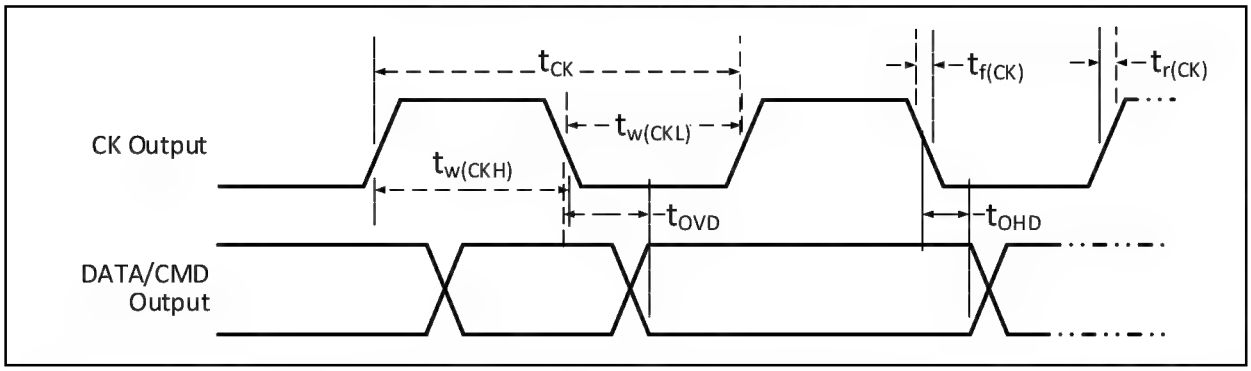


Table 4-30 SD/MMC interface characteristics

Symbol	Parameter	Condition		Min.	Max.	Unit
f_{CK}/t_{CK}	Clock frequency in data transfer mode	CL≤30pF			48	MHz
$t_{W(CKL)}$	Clock low time	CL≤30pF		6		ns
$t_{W(CKH)}$	Clock high time	CL≤30pF		6		
$t_{r(CK)}$	Rise Time	CL≤30pF			4	
$t_{f(CK)}$	Fall time	CL≤30pF			4	
CMD/DAT input (refer to CK)						
t_{ISU}	Input setup time	CL≤30pF		7		ns
t_{IH}	Input hold time	CL≤30pF		2		
CMD/DAT output in high-speed mode (refer to CK)						
t_{OV}	Output valid time	CL≤30pF	Master mode		5	ns
			Slave mode		9	
t_{OH}	Output hold time	CL≤30pF		20		
CMD/DAT output in default mode (refer to CK)						
t_{OVD}	Output valid default time	CL≤30pF	Master mode		8	ns
			Slave mode		14	
t_{OHD}	Output hold default time	CL≤30pF		20		

4.3.18 FSMC Characteristics

Figure 4-16 Asynchronous multiplexed PSRAM/NOR read waveform

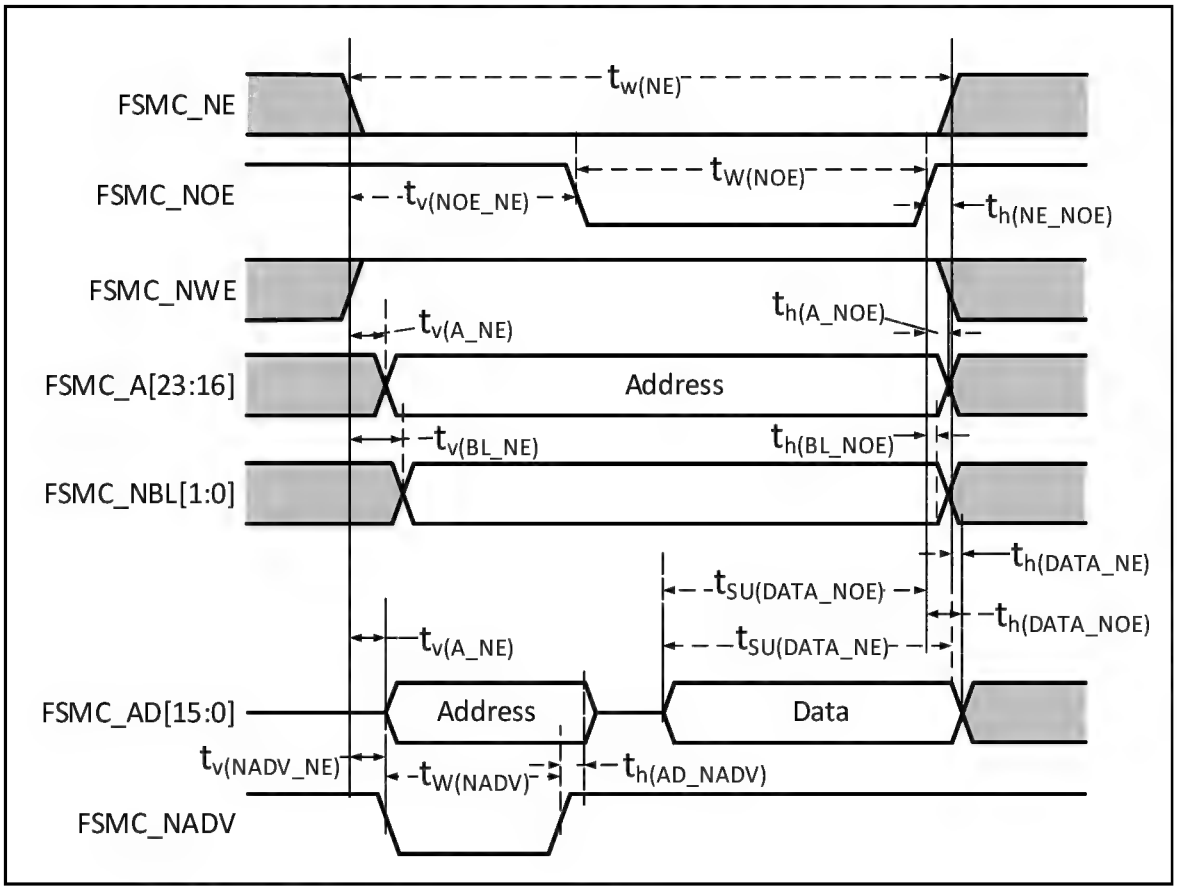


Table 4-31 Asynchronous multiplexed PSRAM/NOR read timings

Symbol	Parameter	Min.	Max.	Unit
$t_{W(NE)}$	FSMC_NE low time	$7t_{HCLK}$		ns
$t_{V(NOE_NE)}$	FSMC_NE low to FSMC_NOE low	0		
$t_{W(NOE)}$	FSMC_NOE low time	$7t_{HCLK}$		
$t_{h(NE_NOE)}$	FSMC_NOE high to FSMC_NE high hold time	0		
$t_{V(A_NE)}$	FSMC_NE low to FSMC_A valid	0	5	
$t_{V(NADV_NE)}$	FSMC_NE low to FSMC_NADV low	0	5	
$t_{W(NADV)}$	FSMC_NADV low time	t_{HCLK}		
$t_{h(AD_NADV)}$	FSMC_AD (address) valid hold time after FSMC_NADV high	$2t_{HCLK}$		
$t_{h(A_NOE)}$	Address hold time after FSMC_NOE high	0		
$t_{h(BL_NOE)}$	FSMC_BL hold time after FSMC_NOE high	0		
$t_{V(BL_NE)}$	FSMC_NE low to FSMC_BL valid	0	5	
$t_{SU(DATA_NE)}$	Data to FSMC_NE high setup time	$3t_{HCLK}$		
$t_{SU(DATA_NOE)}$	Data to FSMC_NOE high setup time	$3t_{HCLK}$		
$t_{h(DATA_NE)}$	Data hold time after FSMC_NE high	0		
$t_{h(DATA_NOE)}$	Data hold time after FSMC_NOE high	0		

Figure 4-17 Asynchronous multiplexed PSRAM/NOR write waveform

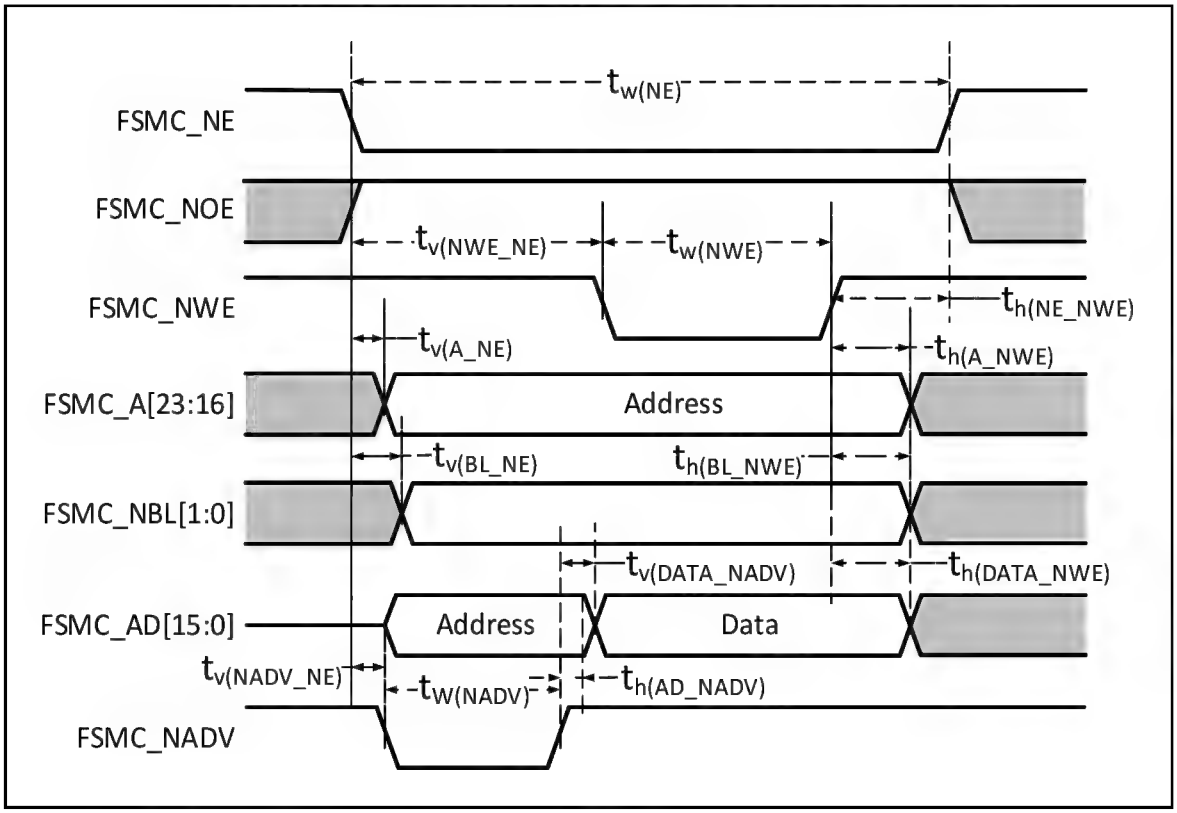


Table 4-32 Asynchronous multiplexed PSRAM/NOR write timings

Symbol	Parameter	Min.	Max.	Unit
$t_{W(NE)}$	FSMC_NE low time	$5t_{HCLK}$		ns
$t_{V(NEW_NE)}$	FSMC_NE low to FSMC_NWE low	$3t_{HCLK}$		
$t_{W(NWE)}$	FSMC_NWE low time	$2t_{HCLK}$		
$t_{h(NE_NWE)}$	FSMC_NWE high to FSMC_NE high hold time	t_{HCLK}		
$t_{V(A_NE)}$	FSMC_NE low to FSMC_A valid	0	5	
$t_{V(NADV_NE)}$	FSMC_NE low to FSMC_NADV low	0	5	
$t_{W(NADV)}$	FSMC_NADV low time	t_{HCLK}		
$t_{h(AD_NADV)}$	FSMC_AD (address) valid hold time after FSMC_NADV high	$2t_{HCLK}$		
$t_{h(A_NWE)}$	Address hold time after FSMC_NWE high	t_{HCLK}		
$t_{V(BL_NE)}$	FSMC_NE low to FSMC_BL valid	0	5	
$t_{h(BL_NWE)}$	FSMC_BL hold time after FSMC_NWE high	t_{HCLK}		
$t_{V(DATA_NADV)}$	FSMC_NADV high to data hold time	$2t_{HCLK}$		
$t_{h(DATA_NWE)}$	Data hold time after FSMC_NWE high	t_{HCLK}		

Figure 4-18 Synchronous multiplexed NOR/PSRAM read waveform

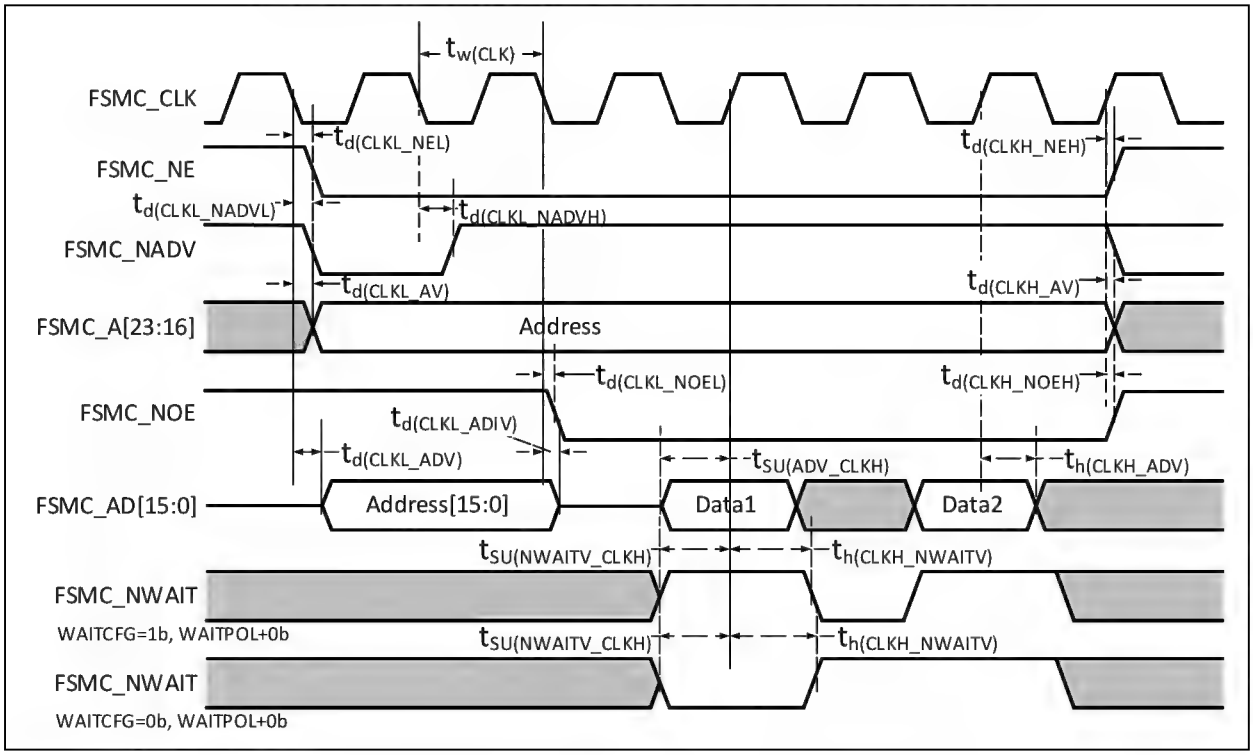


Table 4-33 Synchronous multiplexed NOR/PSRAM read timings

Symbol	Parameter	Min.	Max.	Unit
$t_{W(CLK)}$	FSMC_CLK period	$2t_{HCLK}$		ns
$t_{d(CLKL_NEL)}$	FSMC_CLK low to FSMC_NE low	0	5	
$t_{d(CLKH_NEH)}$	FSMC_CLK high to FSMC_NE high	$0.5t_{HCLK}$	$0.5t_{HCLK}$	
$t_{d(CLKL_NADVL)}$	FSMC_CLK low to FSMC_NADV low	0	5	
$t_{d(CLKL_NADVH)}$	FSMC_CLK low to FSMC_NADV high	0	5	
$t_{d(CLKL_AV)}$	FSMC_CLK low to FSMC_Ax valid (x = 16…23)	0	5	
$t_{d(CLKH_AIV)}$	FSMC_CLK high to FSMC_Ax invalid (x = 16…23)	0	5	
$t_{d(CLKL_NOEL)}$	FSMC_CLK low to FSMC_NOE low	$2t_{HCLK}$		
$t_{d(CLKH_NOEH)}$	FSMC_CLK high to FSMC_NOE high	t_{HCLK}		
$t_{d(CLKL_ADV)}$	FSMC_CLK low to FSMC_AD[15:0] valid	0	5	
$t_{d(CLKL_ADIV)}$	FSMC_CLK low to FSMC_AD[15:0] invalid	0	5	
$t_{SU(ADV_CLKH)}$	FSMC_AD[15:0] valid data before FSMC_CLK high	8		
$t_{h(CLKH_ADV)}$	FSMC_AD[15:0] valid data after FSMC_CLK high	8		
$t_{SU(NWAITV_CLKH)}$	FSMC_NWAIT valid before FSMC_CLK high	6		
$t_{h(CLKH_NWAITV)}$	FSMC_NWAIT valid after FSMC_CLK high	2		

Figure 4-19 Synchronous multiplexed PSRAM write waveform

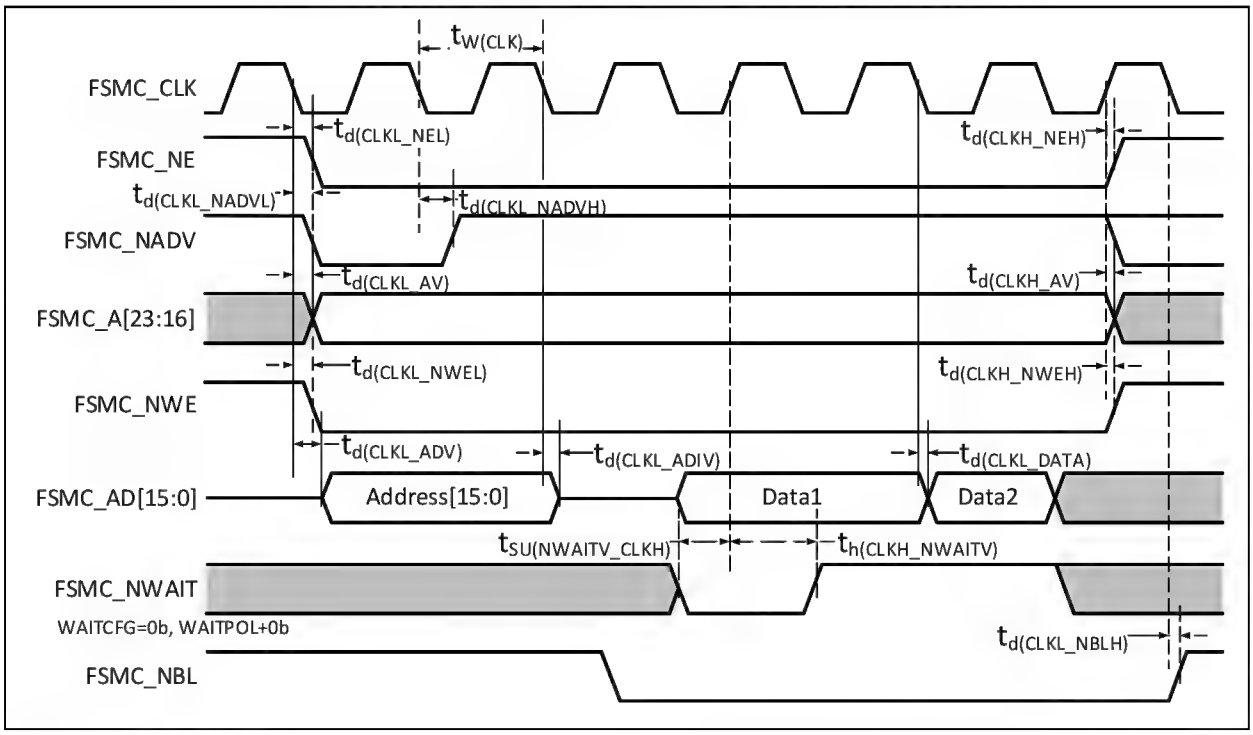


Table 4-34 Synchronous multiplexed PSRAM write timings

Symbol	Parameter	Min.	Max.	Unit
$t_{W(CLK)}$	FSMC_CLK period	$2t_{HCLK}$		ns
$t_{d(CLKL_NEL)}$	FSMC_CLK low to FSMC_NE low	0	5	
$t_{d(CLKH_NEH)}$	FSMC_CLK high to FSMC_NE high	$0.5t_{HCLK}$	$0.5t_{HCLK}$	
$t_{d(CLKL_NADVL)}$	FSMC_CLK low to FSMC_NADV low	0	5	
$t_{d(CLKL_NADVH)}$	FSMC_CLK low to FSMC_NADV high	0	5	
$t_{d(CLKL_AV)}$	FSMC_CLK low to FSMC_Ax valid (x = 16…23)	0	5	
$t_{d(CLKH_AIV)}$	FSMC_CLK high to FSMC_Ax invalid (x = 16…23)	0	5	
$t_{d(CLKL_NWEL)}$	FSMC_CLK low to FSMC_NWE low	0		
$t_{d(CLKH_NWEH)}$	FSMC_CLK high to FSMC_NWE high	0		
$t_{d(CLKL_ADV)}$	FSMC_CLK low to FSMC_AD[15:0] valid	0	5	
$t_{d(CLKL_ADIV)}$	FSMC_CLK low to FSMC_AD[15:0] invalid	0	5	
$t_{d(CLKL_DATA)}$	FSMC_AD[15:0] valid after FSMC_CLK low	2		
$t_{SU(NWAITV_CLKH)}$	FSMC_NWAIT valid before FSMC_CLK high	6		
$t_{h(CLKH_NWAITV)}$	FSMC_NWAIT valid after FSMC_CLK high	2		
$t_{d(CLKL_NBLH)}$	FSMC_CLK low to FSMC_NBL high	2		

NAND controller waveform and timing

Test conditions: NAND operation area, 16-bit data width is selected, ECC calculation circuit is enabled, 512-byte page size, other timing configurations are setting registers FSMC_PCR2=0x0002005E, FSMC_PMEM2=0x01020301, FSMC_PATT2=0x01020301.

Figure 4-20 NAND controller read waveform

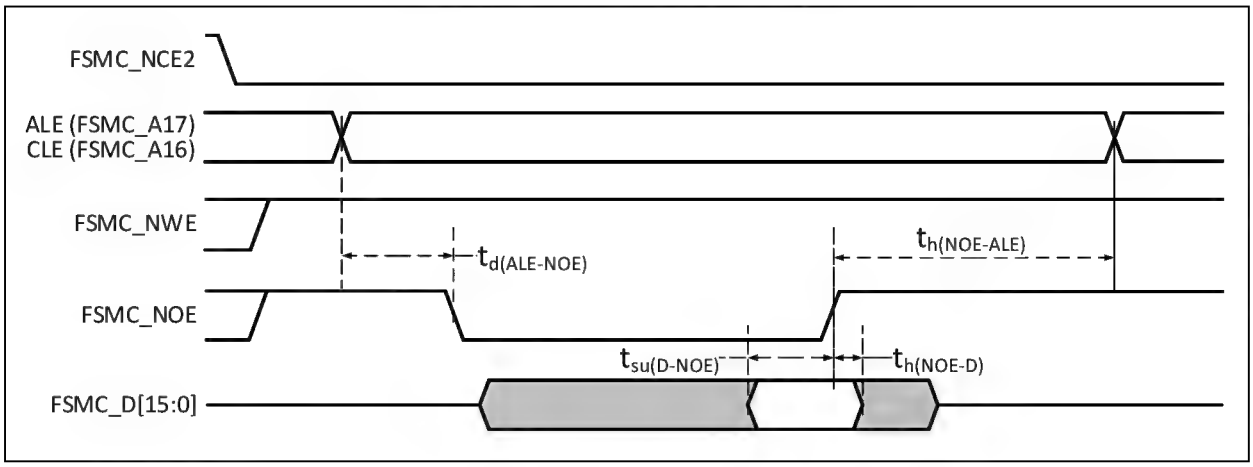


Figure 4-21 NAND controller write waveform

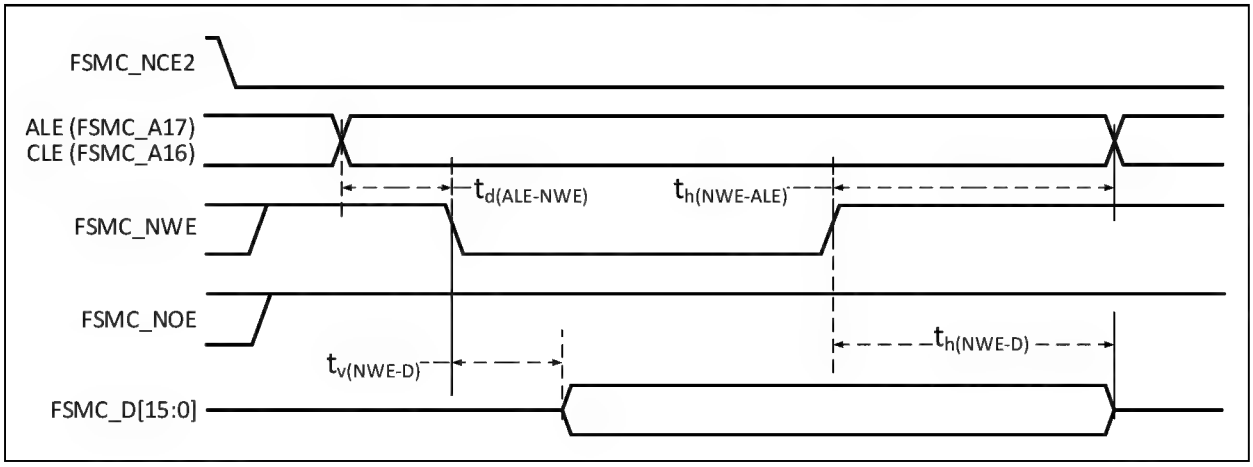


Figure 4-22 NAND controller read waveform in general-purpose storage space

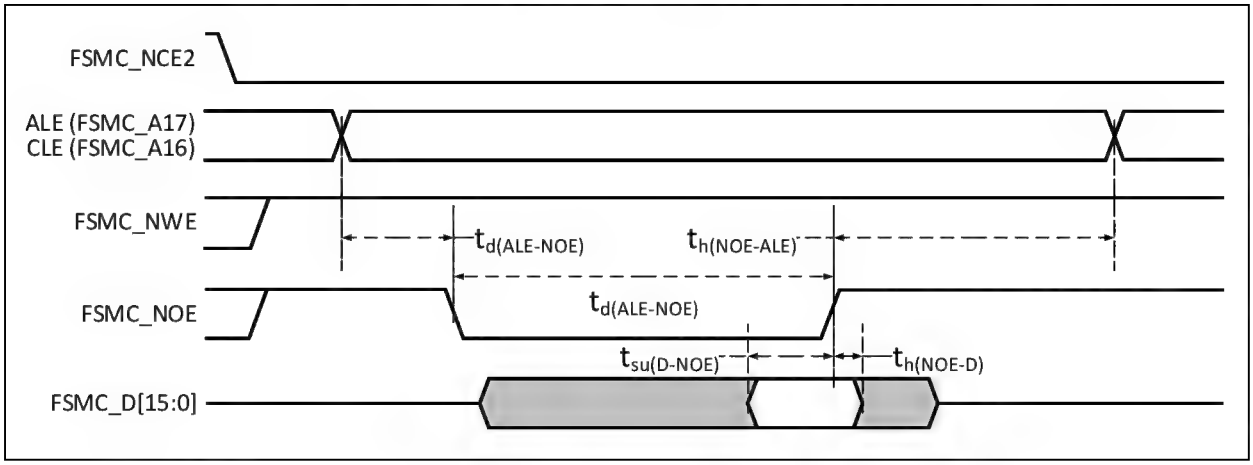


Figure 4-23 NAND controller write waveform in general-purpose storage space

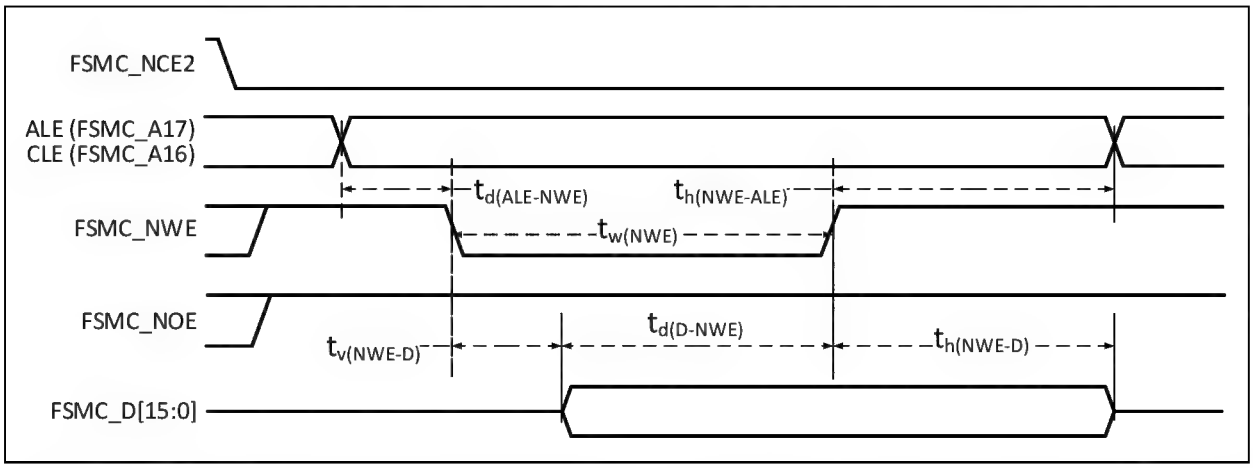


Table 4-35 Timing characteristics of NAND Flash read and write cycles

Symbol	Parameter	Min.	Max.	Unit
$t_{d(D-NWE)}$	Before FSMC_NWE high to FSMC_D[15:0] data valid	$4t_{HCLK}$		ns
$t_{w(NOE)}$	FSMC_NOE low time	$4t_{HCLK}$		
$t_{su(D-NOE)}$	Before FSMC_NOE high to FSMC_D[15:0] data valid	20		
$t_{h(NOE-D)}$	After FSMC_NOE high to FSMC_D[15:0] data valid	15		
$t_{w(NWE)}$	FSMC_NWE low time	$4t_{HCLK}$		
$t_{v(NWE-D)}$	FSMC_NWE low to FSMC_D[15:0] data valid	0		
$t_{h(NWE-D)}$	FSMC_NWE high to FSMC_D[15:0] data invalid	$2t_{HCLK}$		
$t_{d(ALE-NWE)}$	Before FSMC_NWE low to FSMC_ALE valid	$2t_{HCLK}$		
$t_{h(NWE-ALE)}$	FSMC_NWE high to FSMC_ALE invalid	$2t_{HCLK}$		
$t_{d(ALE-NOE)}$	Before FSMC_NOE low to FSMC_ALE valid	$2t_{HCLK}$		
$t_{h(NOE-ALE)}$	FSMC_NOE high to FSMC_ALE invalid	$4t_{HCLK}$		

4.3.19 DVP Interface Characteristics

Figure 4-24 DVP timing waveform

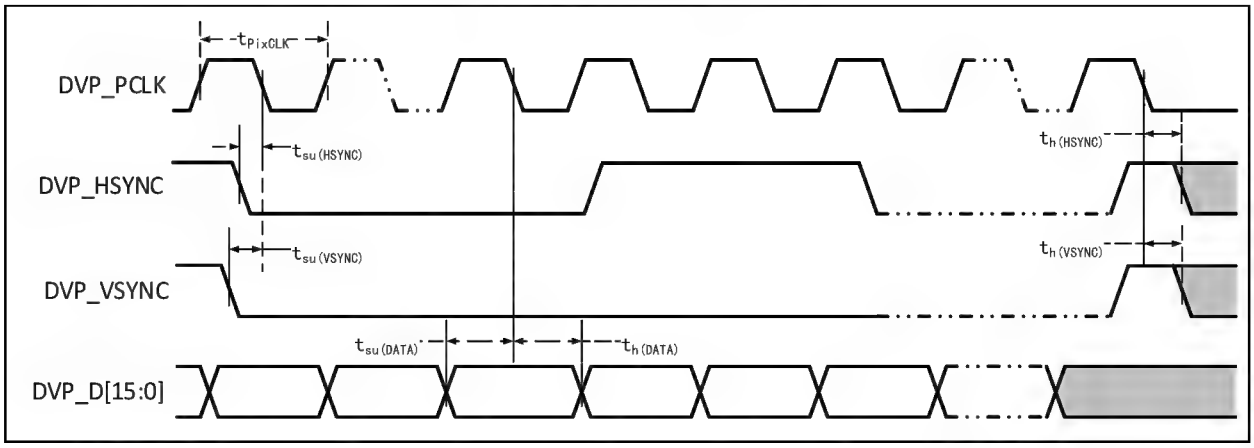


Table 4-36 DVP characteristics

Symbol	Parameter	Min.	Max.	Unit
f_{PixCLK}/t_{PixCLK}	Pixel clock input frequency		144	MHz
$Duty_{(PixCLK)}$	Pixel clock duty cycle	15		%
$t_{su(DATA)}$	Data setup time	2.5		ns
$t_{h(DATA)}$	Data hold time	1		
$t_{su(HSYNC)}/t_{su(VSYNC)}$	HSYNC/VSYNC signal input setup time	2.5		
$t_{h(HSYNC)}/t_{h(VSYNC)}$	HSYNC/VSYNC signal input hold time	1		

4.3.20 Gigabit Ethernet Interface Characteristics

Figure 4-25 ETH-SMI timing waveform

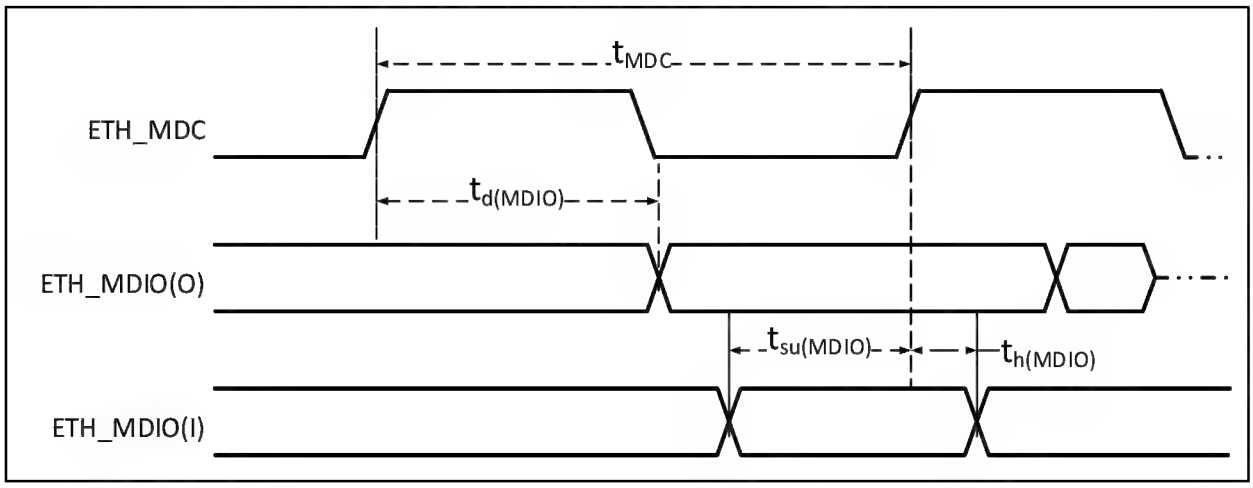


Table 4-37 SMI signal characteristics of Ethernet MAC

Symbol	Parameter	Min.	Typ.	Max.	Unit
f_{MDC}/t_{MDC}	MDC clock frequency			2.5	MHz
$t_{d(MDIO)}$	MDIO write data valid time	0		300	ns
$t_{su(MDIO)}$	Read data setup time	10			
$t_{h(MDIO)}$	Read data hold time	10			

Figure 4-26 ETH-RMII signal timing waveform

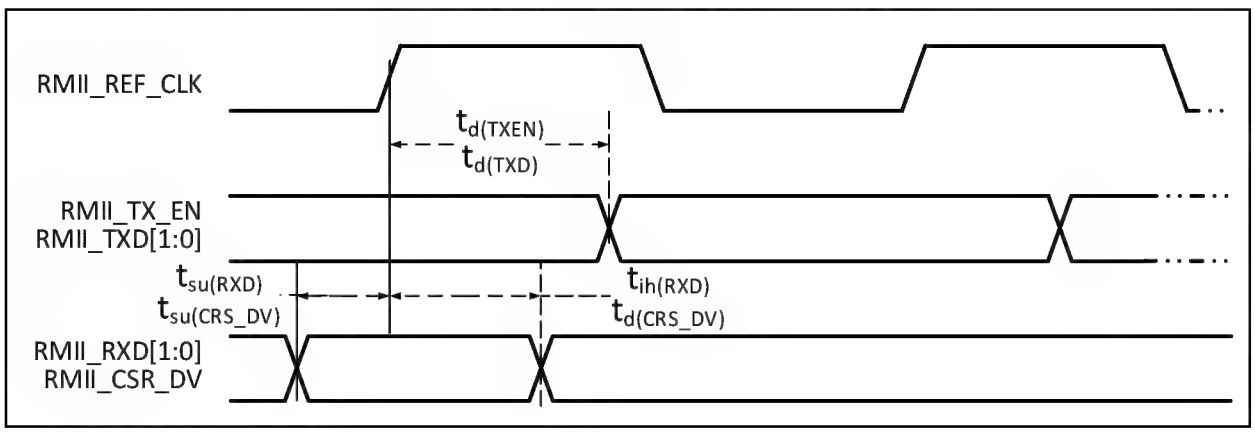


Table 4-38 RMII signal characteristics of Ethernet MAC

Symbol	Parameter	Min.	Typ.	Max.	Unit
$t_{su(RXD)}$	Setup time of received data	4			ns
$t_{ih(RXD)}$	Hold time of received data	2			
$t_{su(CRS_DV)}$	Carrier detect signal setup time	4			
$t_{ih(CRS_DV)}$	Carrier detect signal hold time	2			
$t_{d(TXEN)}$	Transmission enable effective delay time			16	
$t_{d(TXD)}$	Data transmission effective delay time			16	

Figure 4-27 ETH-MII signal timing waveform

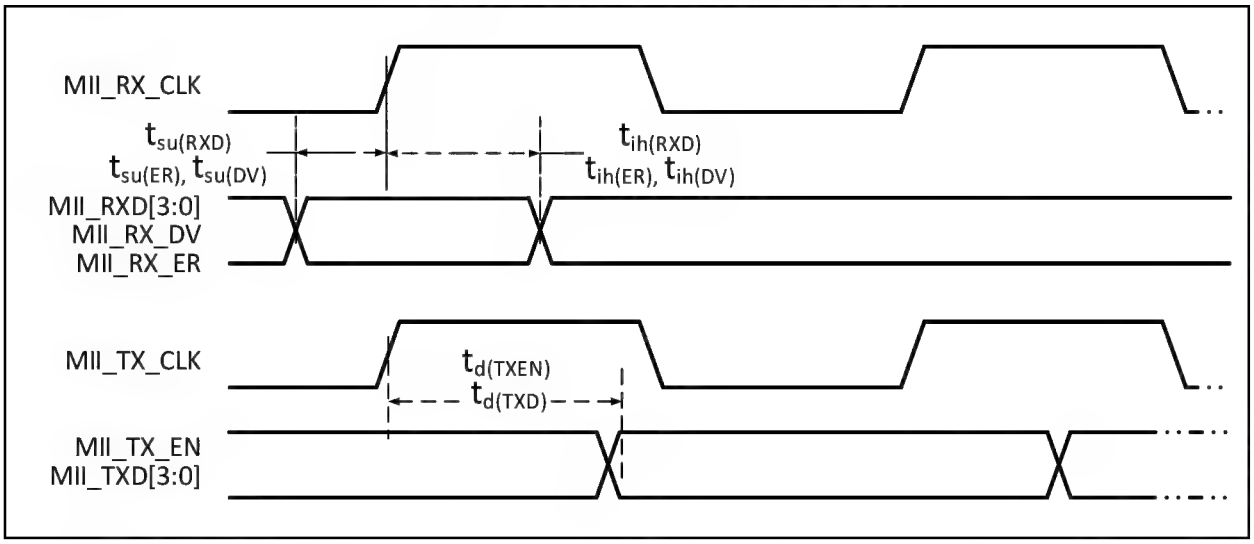


Table 4-39 MII signal characteristics of Ethernet MAC

Symbol	Parameter	Min.	Typ.	Max.	Unit
$t_{su(RXD)}$	Setup time of received data	10			ns
$t_{ih(RXD)}$	Hold time of received data	10			
$t_{su(DV)}$	Data valid signal setup time	10			
$t_{ih(DV)}$	Data valid signal hold time	10			
$t_{su(ER)}$	Error signal setup time	10			
$t_{ih(ER)}$	Error signal hold time	10			
$t_{d(TXEN)}$	Transmission enable effective delay time			16	
$t_{d(TXD)}$	Data transmission effective delay time			16	

Figure 4-28 ETH-RGMII signal timing waveform

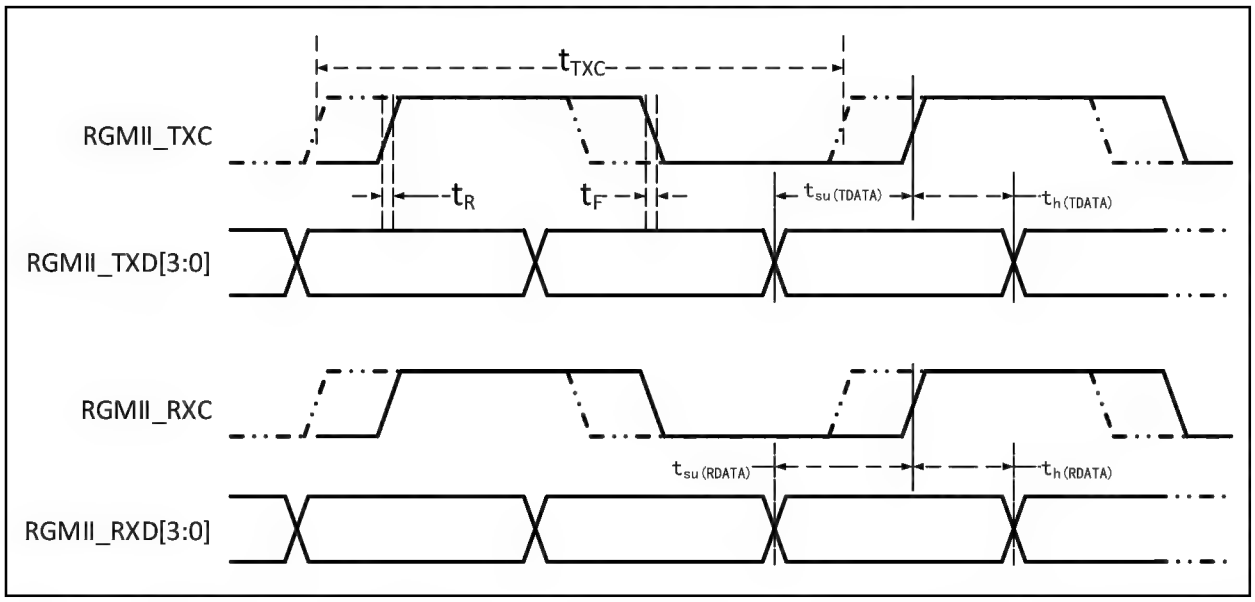


Table 4-40 RGMII signal characteristics of Ethernet MAC

Symbol	Parameter	Min.	Typ.	Max.	Unit
f_{TXC}/t_{TXC}	TXC/RXC clock frequency	7.2	8	8.8	ns
t_R	TXC/RXC rise time			2.0	
t_F	TXC/RXC fall time			2.0	
$t_{su(TDATA)}$	Transmit data setup time	1.2	2.0		
$t_{h(TDATA)}$	Transmit data hold time	1.2	2.0		
$t_{su(RDATA)}$	Input data setup time	1.2	2.0		
$t_{h(RDATA)}$	Input data hold time	1.2	2.0		

4.3.21 12-bit ADC Characteristics

Table 4-41 ADC characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DDA}	Supply voltage		2.4		3.6	V
V_{REF+}	Positive reference voltage	V_{REF+} cannot be more than V_{DDA}	2.4		V_{DDA}	V
I_{VREF}	Reference current			160	220	uA
I_{DDA}	Supply current			480	530	uA
f_{ADC}	ADC clock frequency				14	MHz
f_S	Sampling rate		0.05		1	MHz
f_{TRIG}	External trigger frequency				16	$1/f_{ADC}$
V_{AIN}	Conversion voltage range		0		V_{REF+}	V
R_{AIN}	External input impedance				50	kΩ
R_{ADC}	Sampling switch resistance			0.6	1	kΩ
C_{ADC}	Internal sample and hold capacitor			8		pF

t_{CAL}	Calibration time			40		$1/f_{ADC}$
t_{Iat}	Injected trigger conversion latency				2	$1/f_{ADC}$
t_{Iatr}	Regular trigger conversion latency				2	$1/f_{ADC}$
t_s	Sampling time		1.5		239.5	$1/f_{ADC}$
t_{STAB}	Power-on time				1	us
t_{CONV}	Total conversion time (including sampling time)		14		252	$1/f_{ADC}$

Note: Above parameters are guaranteed by design.

Formula: Maximum R_{AIN}

$$R_{AIN} < \frac{Ts}{f_{ADC} \times C_{ADC} \times \ln 2^{N+2}} - R_{ADC}$$

The above formula is used to determine the maximum external impedance so that the error can be less than 1/4 LSB. Where N=12 (representing 12-bit resolution).

Table 4-42 Maximum RAIN when f_{ADC} = 14MHz

T_S(cycle)	t_S (us)	Maximum R_{AIN}(kΩ)
1.5	0.11	0.4
7.5	0.54	5.9
13.5	0.96	11.4
28.5	2.04	25.2
41.5	2.96	37.2
55.5	3.96	50
71.5	5.11	Invalid
239.5	17.1	Invalid

Table 4-43 ADC error

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
EO	Offset error	f_{PCLK2} = 56MHz, f_{ADC} = 14MHz, R_{AIN} < 10kΩ, V_{DDA} = 3.3V		±4		LSB
ED	Differential nonlinearity error			±0.5	±3	
EL	Integral nonlinearity error			±1	±4	

C_p represents the parasitic capacitance on the PCB and the pad (about 5pF), which may be related to the quality of the pad and PCB layout. A larger C_p value will reduce the conversion accuracy, the solution is to reduce the f_{ADC} value.

Figure 4-29 ADC typical connection diagram

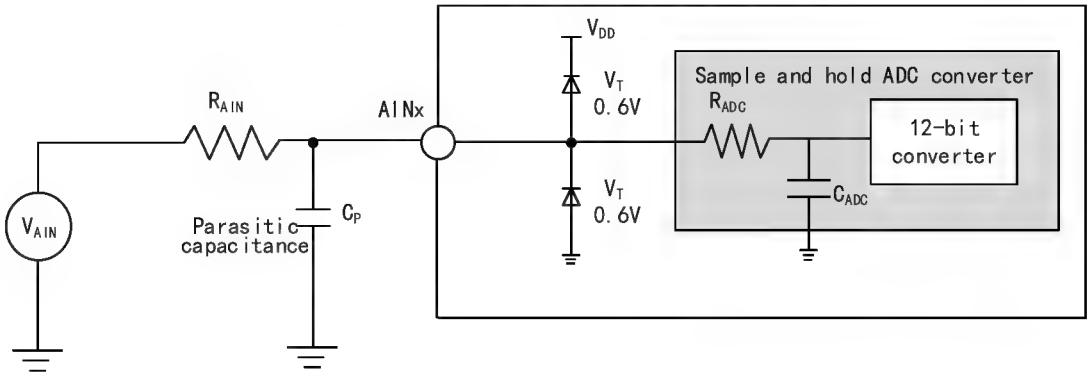
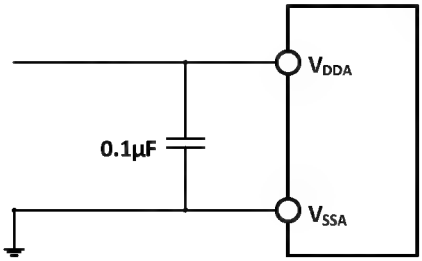


Figure 4-30 Analog power supply and decoupling circuit reference



4.3.22 Temperature Sensor Characteristics

Table 4-44 Temperature sensor characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
R_{TS}	Measurement range of temperature sensor		-40		85	℃
A_{TSC}	Measurement range of temperature sensor after software calibration			±12		℃
Avg_Slope	Average slope (negative temperature coefficient)		3.8	4.3	4.7	mV/℃
V_{25}	Voltage at 25℃		1.34	1.40	1.46	V
T_{S_temp}	ADC sampling time when reading temperature	f_{ADC} = 14MHz			17.1	us

4.3.23 DAC Characteristics

Table 4-45 DAC characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DDA}	Supply voltage		2.4	3.3	3.6	V
V_{REF+}	Positive reference voltage	$V_{REF+} \leq V_{DDA}$	2.4	3.3	3.6	V
R_L(1)	Resistive load with buffer ON		5			kΩ
	Resistive load with buffer OFF		15			kΩ
C_L(1)	Capacitive load with buffer ON				50	pF

V_{OUT_MIN}(1)	12-bit DAC conversion with buffer ON		0		8	mV
V_{OUT_MAX}(1)		VREF+=3.3V	3.29		3.3	V
V_{OUT_MIN}(1)	12-bit DAC conversion with buffer OFF		0		3	mV
V_{OUT_MAX}(1)		VREF+=3.3V	3.295		3.3	V
I_{VREF+}	With no load, 0x800 on the inputs			58		uA
	With no load, 0xF1C at V_{REF+}=3.6V on the inputs			194		
	With no load, 0x555 (worst) at V_{REF+}=3.6V on the inputs			331		
I_{DDA}	With buffer ON and no load, 0x800 on the inputs			170		uA
	With buffer ON and no load, 0xF1C on the inputs at V_{REF+}=3.6V,			150		
	With buffer ON and no load, 0x555 (worst) at V_{REF+}=3.6V on the inputs			170		
DNL	Differential nonlinearity error			±2		LSB
INL	Integral nonlinearity error	After calibration of offset error and gain error		±4		LSB
Offset	Offset error			±3	±12	mV
		V_{REF+}=3.6V			±10	LSB
Gain error		DAC in 12-bit configuration		±0.4		%
Amplifier gain(1)	Amplifier gain in open loop	5kΩ load (max)	80	85		dB
$t_{SETTLING}$	Setting time (full scale: for an input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±1 LSB)	C_{LOAD}≤50pF R_{LOAD}≥5kΩ		3	4	us
Update rate	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB),	C_{LOAD}≤50pF R_{LOAD}≥5kΩ			1	MS/s
t_{WAKEUP}	Time to wake up from off state (PDV18 changes from 1 to 0)	C_{LOAD}≤50pF, R_{LOAD}≥5kΩ, input codes between the lowest and highest possible ones		6.5	10	us
PSRR+(1)	Power supply rejection ratio (relative to V_{DDA}) (static DC measurement)	No R_{LOAD}, C_{LOAD}≤50pF		-100	-75	dB

Note: 1. Guaranteed by design, not tested in production.

4.3.24 OPA Characteristics

Table 4-46-1 OPA characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DDA}	Supply voltage		2.4	3.3	3.6	V
C_{MIR}	Common mode input voltage		0		V_{DDA}	V
O_{SW}(3)	Output swing		0		V_{DDA}	V
$V_{IOFFSET}$	Input offset voltage			±2.5	±10	mV
I_{LOAD}	Drive current				600	uA
$I_{DDOPAMP}$	Current consumption	No load, static mode		195		uA
C_{MRR}(1)	Common mode rejection ratio	@1kHz		96		dB
P_{SRR}(1)	Power supply rejection ratio	@1kHz		86		dB
A_V(1)	Open loop gain	C_{LOAD}=5pF		136		dB
G_{BW}(1)	Unit gain bandwidth	C_{LOAD}=5pF		19		MHz
P_M(1)	Phase margin	C_{LOAD}=5pF		93		°
S_R(1)	Slew rate limited	C_{LOAD}=5pF		8		V/us
t_{WAKUP}(1)	Shutdown to wakeup settling time, 0.1%	Input V_{DDA}/2, C_{LOAD} = 50pF, R_{LOAD} = 4kΩ			0.5	us
R_{LOAD}	Resistive load		4			kΩ
C_{LOAD}	Capacitive load				50	pF
V_{OHSAT}(2)	High saturation output voltage	R_{LOAD}=4kΩ, input V_{DDA}	V_{DDA}-300	V_{DDA}-150		mV
		R_{LOAD}=20kΩ, input V_{DDA}	V_{DDA}-50	V_{DDA}-30		
V_{OLSAT}(2)	Low saturation output voltage	R_{LOAD}=4kΩ, input 0		3	10	mV
		R_{LOAD}=20kΩ, input 0		3	10	
EN(1)	Equivalent input voltage noise	R_{LOAD}=4kΩ,@1kHz		83		$\frac{nv}{\sqrt{Hz}}$
		R_{LOAD}=4kΩ,@10kHz		42		

Note: 1. The source simulation is not a real measurement.

2. The load current limits the saturated output voltage.

3. When pins PE7, PE8, PE14 and PE15 are used for OPA output, their output swing is limited: 0 ≤ O_{SW} ≤ 2V when V_{DDA} = 3.3V.

Table 4-46-2 OPA characteristics (High-speed mode)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DDA}	Supply voltage		2.4	3.3	3.6	V
C_{MIR}	Common mode input voltage		0		V_{DDA}	V
O_{SW}(3)	Output swing		0		V_{DDA}	V
$V_{IOFFSET}$	Input offset voltage			±2.5	±10	mV
I_{LOAD}	Drive current				600	uA
$I_{DDOPAMP}$	Current consumption	No load, static mode		770		uA
C_{MRR}(1)	Common mode rejection ratio	@1kHz		96		dB

P_{SRR}(1)	Power supply rejection ratio	@1kHz		86		dB
A_V(1)	Open loop gain	C_{LOAD} = 5pF		136		dB
G_{BW}(1)	Unit gain bandwidth	C_{LOAD} = 5pF		53		MHz
P_M(1)	Phase margin	C_{LOAD} = 5pF		93		°
S_R(1)	Slew rate limited	C_{LOAD} = 5pF		16		V/us
t_{WAKUP}(1)	Shutdown to wakeup settling time, 0.1%	Input V_{DDA}/2, C_{LOAD} = 50pF, R_{LOAD} = 4kΩ			0.5	us
R_{LOAD}	Resistive load		4			kΩ
C_{LOAD}	Capacitive load				30	pF
V_{OHSAT}(2)	High saturation output voltage	R_{LOAD} = 4kΩ, input V_{DDA}	V_{DDA}-300	V_{DDA}-150		mV
		R_{LOAD} = 20kΩ, input V_{DDA}	V_{DDA}-50	V_{DDA}-30		
V_{OLSAT}(2)	Low saturation output voltage	R_{LOAD} = 4kΩ, input 0		3	10	mV
		R_{LOAD} = 20kΩ, input 0		3	10	
EN(2)	Equivalent input voltage noise	R_{LOAD} = 4kΩ,@1kHz		83		$\frac{nv}{\sqrt{Hz}}$
		R_{LOAD} = 4kΩ,@10kHz		42		

Note: 1. The source simulation is not a real measurement.

2. The load current limits the saturated output voltage.

3. When pins PE7, PE8, PE14 and PE15 are used for OPA output, their output swing is limited: 0 ⩽ O_{SW} ⩽ 2V when V_{DDA} = 3.3V.

Chapter 5 Package and Ordering Information

Packages

Package Form	Body Size	Pin Pitch		Package Description	Packing Type
LQFP48	7*7mm	0.5mm	19.7mil	Low Profile Quad Flat Pack	CH32V303CBT6
LQFP64M	10*10mm	0.5mm	19.7mil	Low Profile Quad Flat Pack	CH32V303RBT6
LQFP64M	10*10mm	0.5mm	19.7mil	Low Profile Quad Flat Pack	CH32V303RCT6
LQFP100	14*14mm	0.5mm	19.7mil	Low Profile Quad Flat Pack	CH32V303VCT6
TSSOP20	4.4*6.5mm	0.65mm	25.6mil	Thin Shrink Small Outline Package	CH32V305FBP6
QFN28	4*4mm	0.4mm	15.7mil	Quad Flat No-Lead Package	CH32V305GBU6
LQFP48	7*7mm	0.5mm	19.7mil	Low Profile Quad Flat Pack	CH32V305CCT6
LQFP64M	10*10mm	0.5mm	19.7mil	Low Profile Quad Flat Pack	CH32V305RBT6
LQFP64M	10*10mm	0.5mm	19.7mil	Low Profile Quad Flat Pack	CH32V307RCT6
QFN68	8*8mm	0.4mm	15.7mil	Quad Flat No-Lead Package	CH32V307WCU6
LQFP100	14*14mm	0.5mm	19.7mil	Low Profile Quad Flat Pack	CH32V307VCT6
QFN68	8*8mm	0.4mm	15.7mil	Quad Flat No-Lead Package	CH32V317WCU6
LQFP100	14*14mm	0.5mm	19.7mil	Low Profile Quad Flat Pack	CH32V317VCT6

Note: All dimensions are in millimeters. The pin center spacing values are nominal values, with no error. Other than that, the dimensional error is not greater than the greater of ±0.2mm or 10%.

Figure 5-1 TSSOP20 package

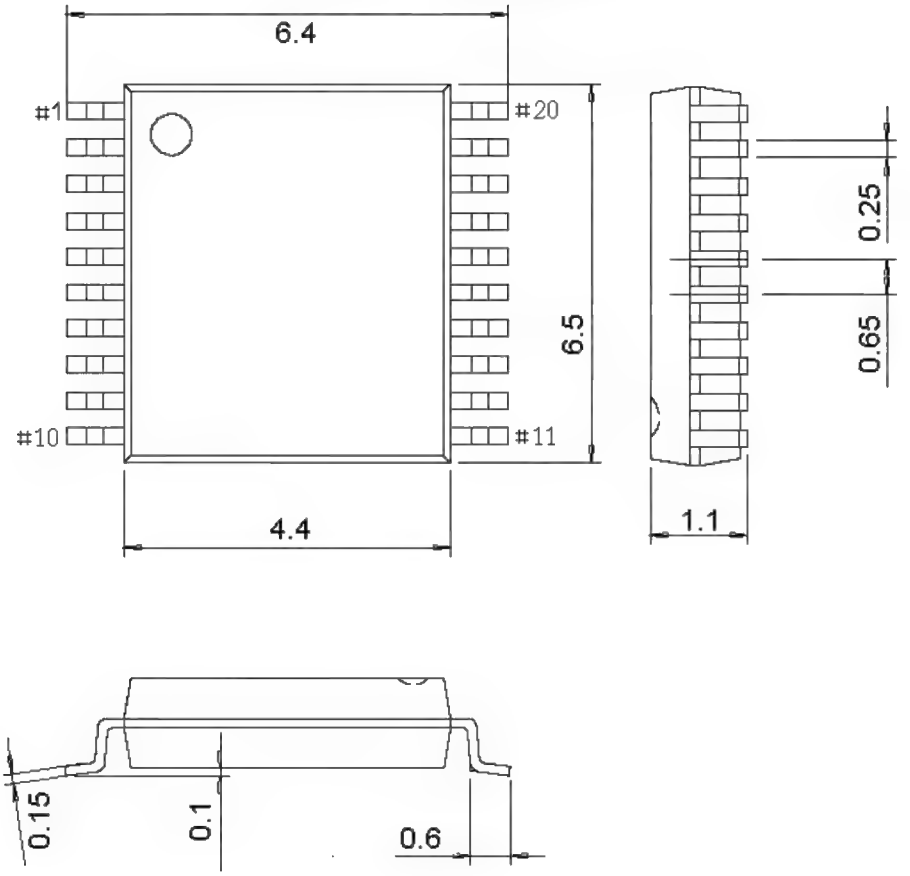


Figure 5-2 QFN28 package

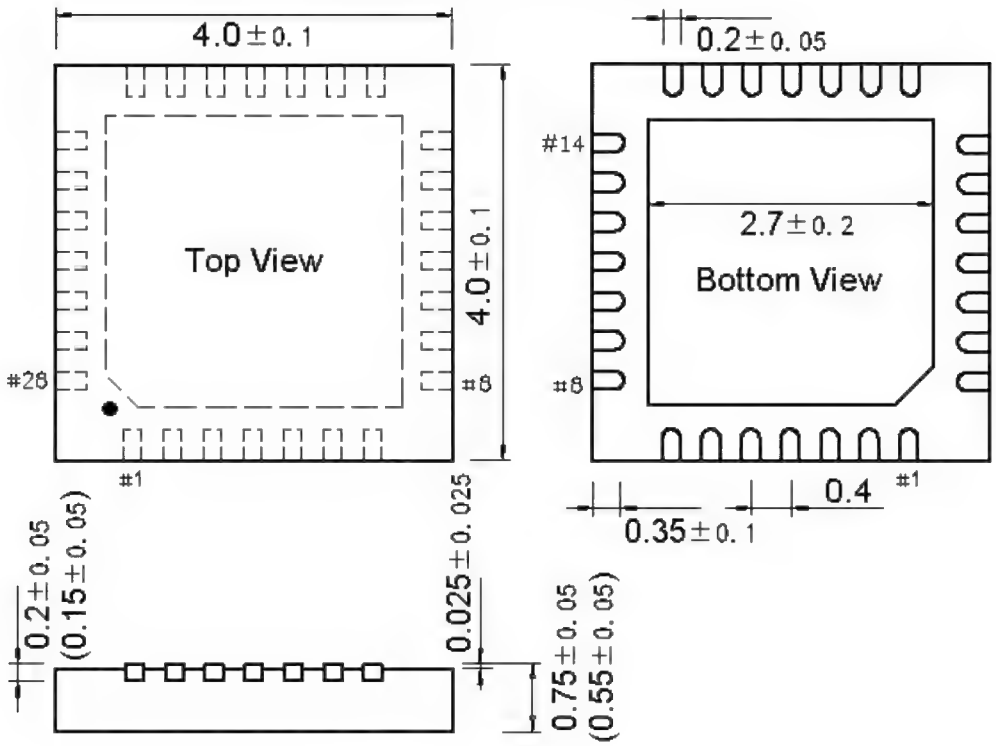


Figure 5-3 LQFP48 package

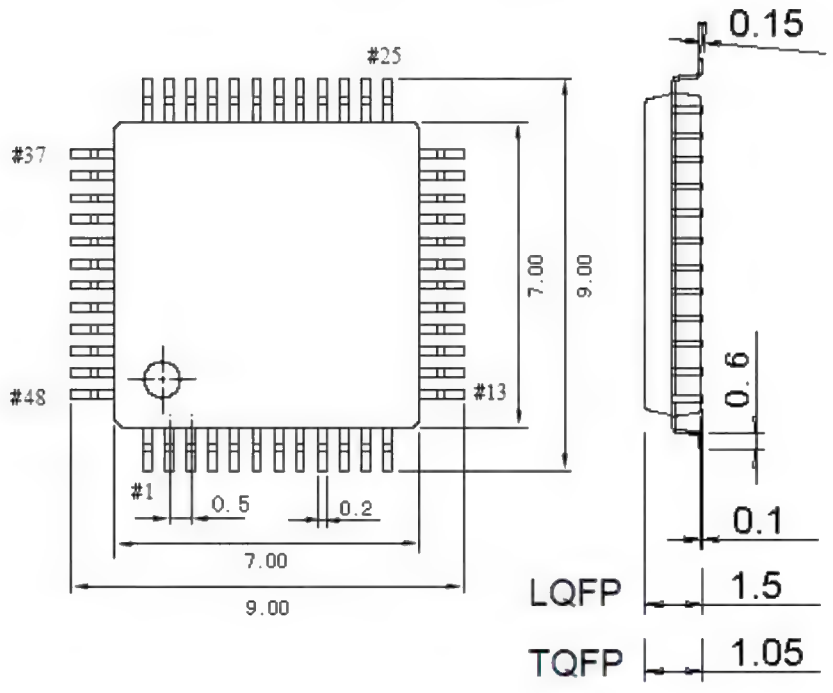


Figure 5-4 LQFP64M package

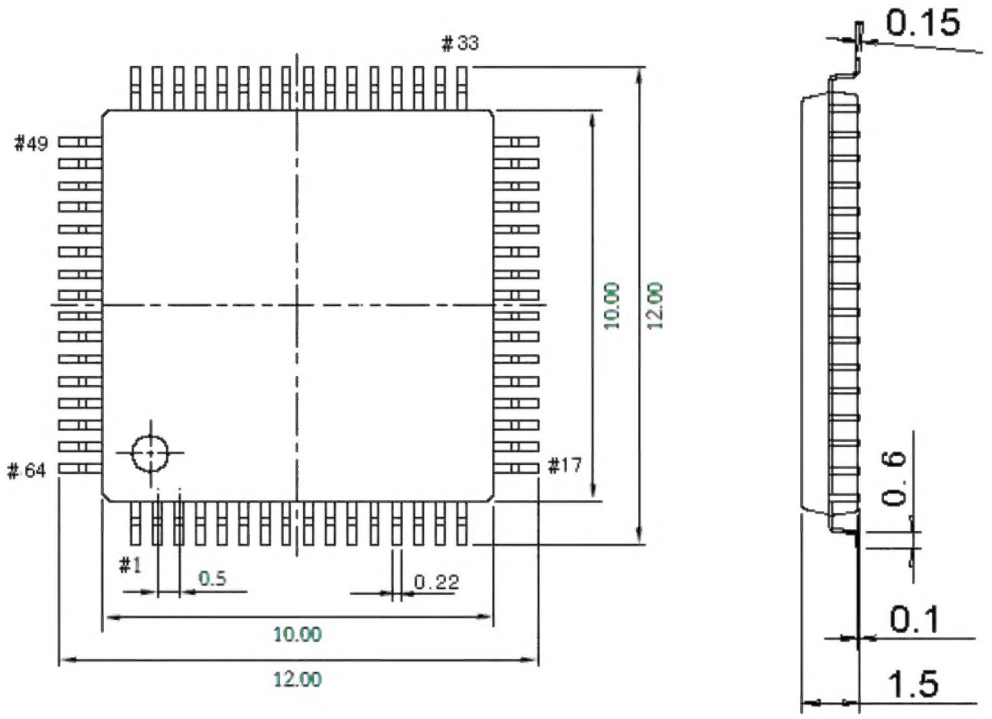


Figure 5-5 QFN68 package

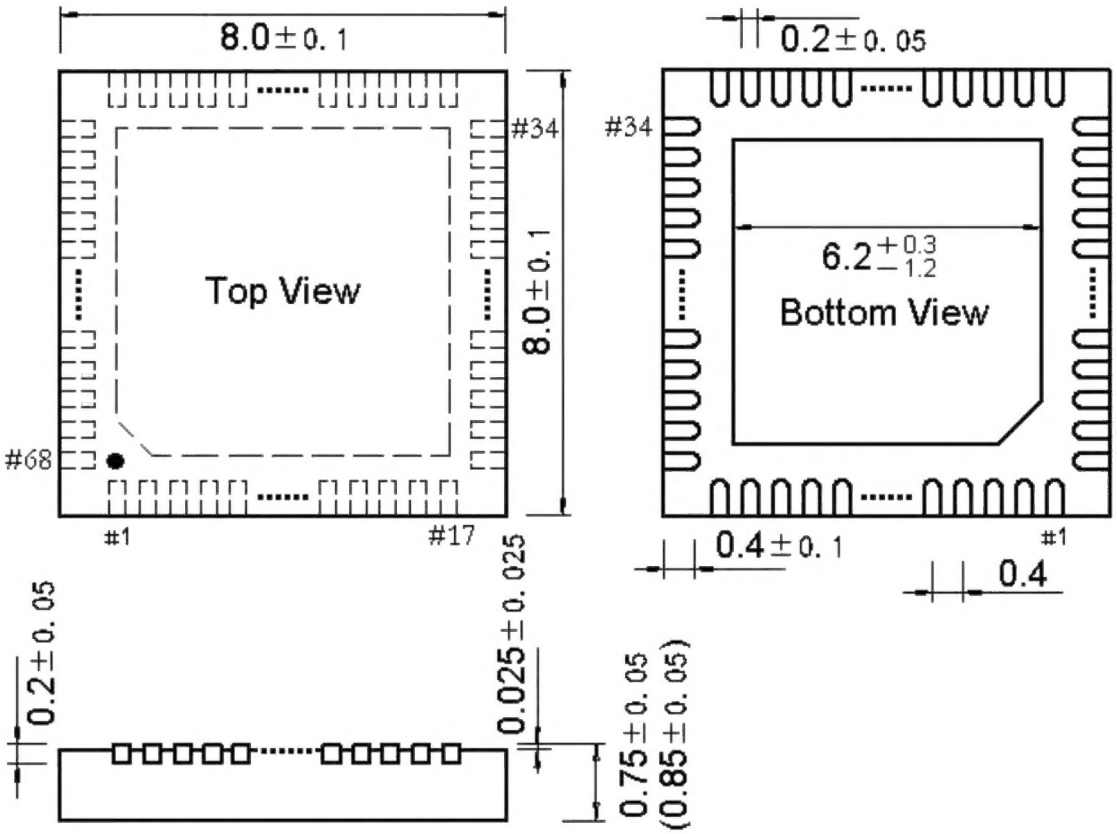
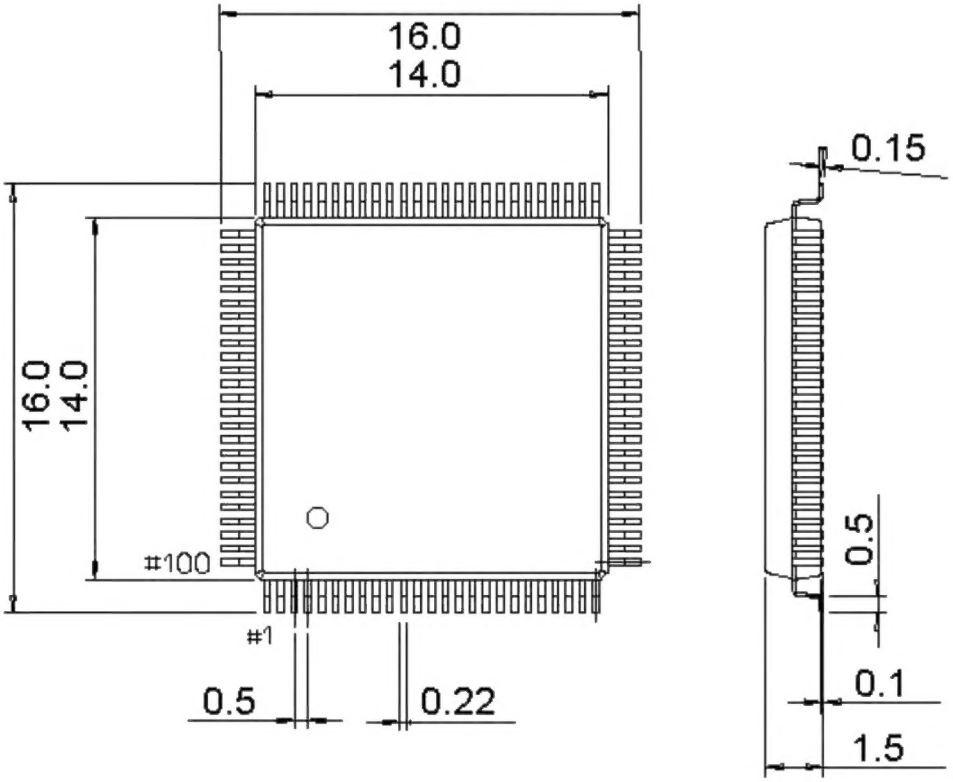


Figure 5-6 LQFP100 package



Series Product Naming Rules

Example: CH32 V 303 R 8 T 6

Device family

F = Arm core, general-purpose MCU

V = QingKe RISC-V core, general-purpose MCU

L = QingKe RISC-V core, low-power MCU

X = QingKe RISC-V core, dedicated or special peripherals MCU

M = QingKe RISC-V core, built-in pre-drive motor MCU

Product type (*) + product subseries (**)

Product type	Product subseries
0 = QingKe V2/V4 core, Super value version, system frequency <=48M	03 = 16K Flash basic general-purpose, OPA 06 = 64K Flash versatile, OPA, dual serial port, TKey 35 = Connection, USB, USB PD/Type-C
1 = M3/QingKe V3/V4 core, Basic version, system frequency<=96M 2 = M3/QingKe V4 non-floating-point core, Enhanced, system frequency <=144M 3 = QingKe V4F floating-point core, Enhanced, system frequency <=144M	03 = Connection, USB 05 = Connection, USB HS, SDIO, CAN 07 = Interconnected, USB HS, CAN, Ethernet, SDIO, FSMC 08 = Wireless, BLE5.x, CAN, USB, Ethernet 17 = Interconnected, USB HS, CAN, Ethernet (built-in PHY), SDIO, FSMC

Pin number

J = 8 pins D = 12 pins A = 16 pins F = 20 pins E = 24 pins

G = 28 pins K = 32 pins T = 36 pins C = 48 pins R = 64 pins

W = 68 pins V = 100 pins Z = 144 pins

Flash memory size

4 = 16K Flash memory 6 = 32K Flash memory 7 = 48K Flash memory

8 = 64K Flash memory B = 128K Flash memory C = 256K Flash memory

Package

T = LQFP U = QFN R = QSOP P = TSSOP M = SOP

Temperature range

6 = -40℃~85℃ (industrial-grade) 7 = -40℃~105℃ (automotive-grade 2)

3 = -40℃~125℃ (automotive-grade 1) D = -40℃~150℃ (automotive-grade 0)